FachHochschule Offenburg University of Applied Sciences

HÄMEEN AMMATTIKORKEAKOULU
Ammatillinen opettajakorkeakoulu

Microphone Beamforming and Audio Signal Processing with TMS320C31 Digital Signal Processor
- Hardware Development -

Diploma Thesis
by

Tobias Kiefer
Damaschkeweg 7
77654 Offenburg / Germany

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Häme Polytechnic Riihimäki / Finland
Department: Information Technology, Option: Telecommunications

University of Applied Sciences Offenburg / Germany
Department: Electrical Engineering and Information Technology
Study Course: Communication Engineering

Supervisors:

T. Karppinen (M.Sc. El. Eng.), Häme Polytechnic / Finland
Professor Dr. (Ing.) W. Reich, FH Offenburg / Germany

OVERVIEW / ÜBERSICHT

This diploma thesis is part of a project for audio signal processing which is using a TMS320C31 microprocessor. With the developed hardware which includes four audio channels and the microprocessor the speech quality should be improved by beamforming.

Each audio channel is using a microphone which receives a speech signal. This will be converted afterwards from analog to digital in order that the microprocessor can process those signals.

In this part of the project is exclusively mentioned the hardware development of the four channel audio board for the pre-processed audio processing and the following analog to digital respectively digital to analog conversion. The main components are the necessary analog filters which are limiting the speech signal in a defined frequency range and the signal conversion which are mentioned above. For both, filter design and printed circuit board development, electrical engineering programs are used. They will be also explained in the following chapters.

Diese Diplomarbeit ist Teil eines Projekts zur Audiosignalverarbeitung mit Hilfe eines TMS320C31 Mikroprozessors. Durch die entwickelte Hardware, die vier Audio Kanäle beinhaltet und den Mikroprozessor, soll die Sprachqualität durch Beamforming verbessert werden.

Dabei wird in jedem Audio Kanal ein Mikrofon verwendet, das Sprachsignale empfängt. Anschließend werden die Signale so aufbereitet, damit diese durch analog / digital Umwandlung dem Mikroprozessor zur weiteren Bearbeitung zur Verfügung gestellt werden können.

In diesem Teil des Projektes wird ausschließlich die Hardware Entwicklung zur benötigten Audiosignalaufbereitung und die anschließenden analog - digital bzw. digital-analog Umwandlungen aufgeführt. Hauptbestandteil sind die einzelnen analogen Filter, die das Sprachsignal in seinem Frequenzbereich begrenzen und die oben schon erwähnten Signalumwandlungen. Sowohl für das Filter Design als auch für die Hardware Entwicklung wurden Programme verwendet, die in den folgenden Kapiteln ebenfalls näher beschrieben werden.

PROLOGUE

Dear reader,

it was a huge opportunity for me to do this diploma thesis abroad, especially in Finland, because I was already studying there last year.
To do this final project work in English was really important for me because afterwards I wanted to study at the Master Degree Program at the University of Applied Sciences Offenburg / Germany.
When I have started with this project at Häme Polytechnic / Finland, everything was new especially the environment. I had no idea what will happen in the following six months. Of course, it has not been easy all the time, there have been some problems and doubts if it is possible to finish this project. But it is not that bad, as an open minded person, I get familiar with everything and I learn how to handle new situations even abroad.

Now, I would like to thank the following persons which have supported me during my work in Finland at the Häme Polytechnic / Finland.
Especially to Timo Karppinen, who offered the project and gave support to me to finish it successfully.
Thanks to Jukka Loimuneva, a teacher at Häme Polytechnic / Finland, who helped me in the field of acoustic and filter development.
Special thanks to Prof. Dr. Reich, who is my supporting professor at the University of Applied Sciences Offenburg / Germany. He has supported me as much as it was possible from Germany.
Thank you for everyone else who is not mentioned explicitly above, but has helped me not only during this project but also in my daily life.

Last but not least I want to thank my parents and all my friends in Germany and in Finland that I had great time in Finland.

Thanks / Danke / Kiitos

ERKLÄRUNG

Hiermit versichere ich eidesstattlich, dass die vorliegende Diplomarbeit von mir selbstständig und ohne unerlaubte fremde Hilfe angefertigt worden ist, insbesondere, dass ich alle Stellen, die wörtlich oder annähernd wörtlich oder dem Gedanken nach aus Veröffentlichungen, unveröffentlichten Unterlagen und Gesprächen entnommen worden sind, als Zitate kenntlich gemacht habe, wobei in den Zitaten jeweils der Umfang der entnommenen Originalzitate kenntlich gemacht wurde. Ich bin mir bewusst, dass eine falsche Versicherung rechtliche Folgen haben wird.

Riihimäki / Finnland, 31.08.2002

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Tobias Kiefer

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TABLE OF CONTENS

TABLE OF CONTENS

1. INTRODUCTION

1.1 Hardware / Project Overview

This diploma thesis contains the hardware development of a Printed Circuit Board (PCB) for microphone beamforming and audio signal processing with a TMS320C31 digital signal processor. The main components for each audio channel of this project are the lowpass filter, Switched Capacitor (SC) bandpass filter, reconstruction filter, A/D Converter, D/A Converter, interfacing to the TMS320C31 microprocessor and a mechanical construction of the four microphones array.

The following Figures 1.1 and 1.2 show a block diagram of each hardware component:

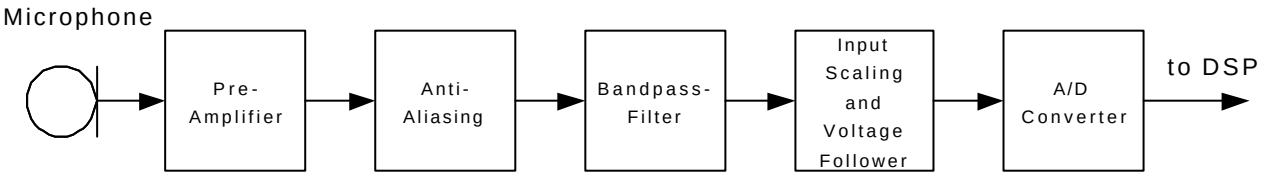


Figure 1.1 Block Diagram in front of DSP

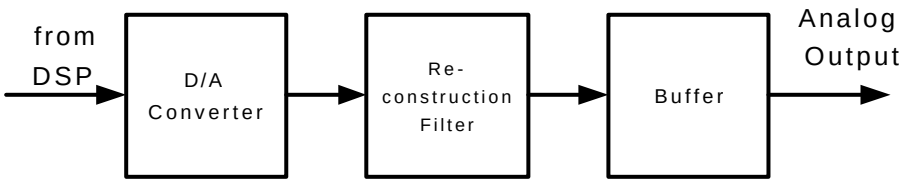


Figure 1.2 Block Diagram behind the DSP

Each part will be described in detail in the following chapters with the theory and practical backgrounds.

The next Figure 1.3 gives the overview of the whole project:

1. INTRODUCTION

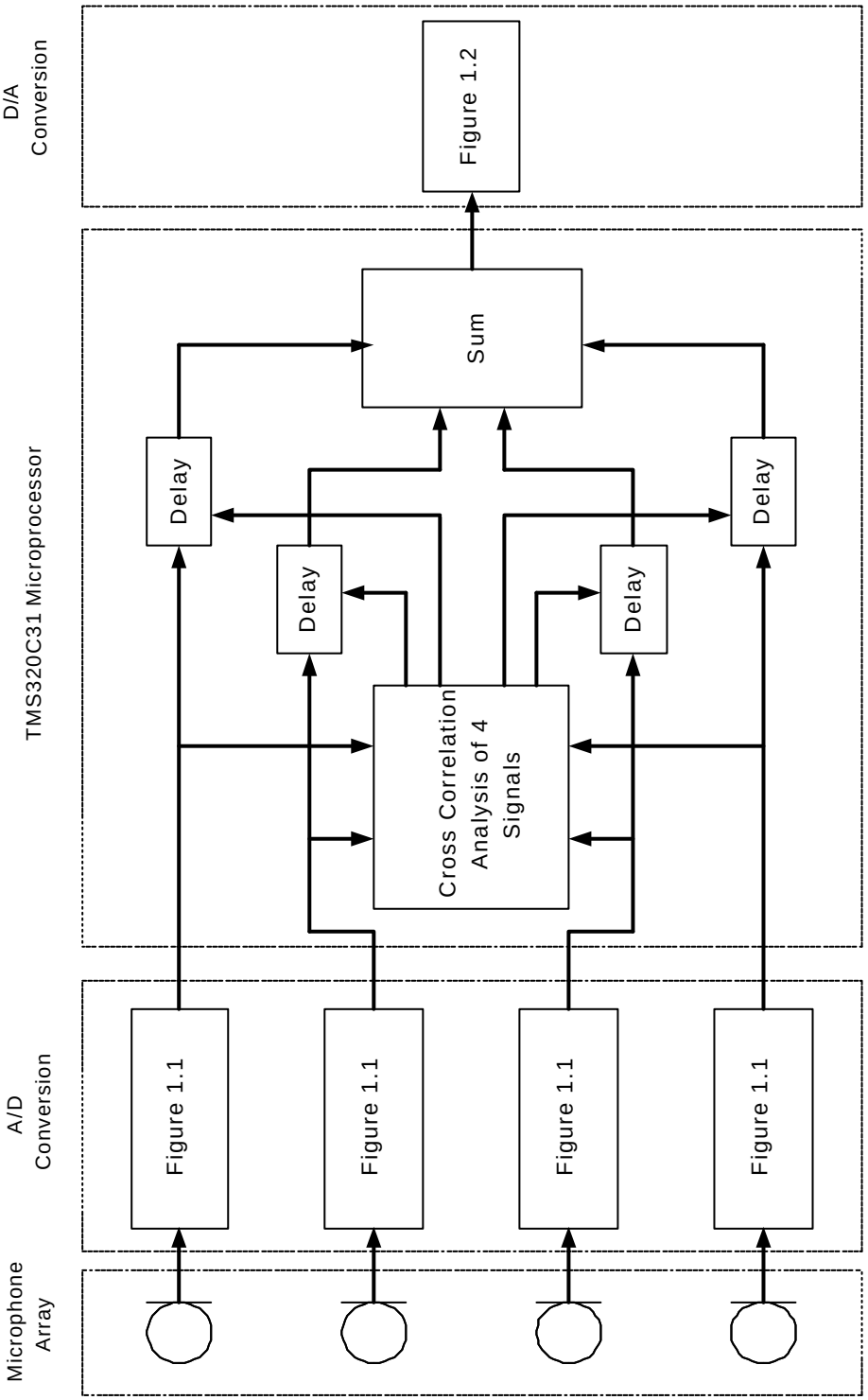


Figure 1.3 General Project Overview

1. INTRODUCTION

This diploma thesis contains the following parts of the whole project which are shown in Figure 1.3:

- *Microphone Array*
- *A/D Conversion*
- *D/A Conversion*

The other section, *TMS320C31 Microprocessor*, is part of another diploma thesis and contains the programming of the TMS320C31 microprocessor and the development of the cross correlation algorithm. The title of this diploma thesis is “Microphone Beamforming and Audio Signal Processing with TMS320C31 Digital Signal Processor - Algorithm and Software Development -.“ [1]
Both projects belong together and can not be considered separately.

1. INTRODUCTION

1.2 Why Beamforming

“In many hands-free speech communication applications, such as audio-conferencing, hands-free mobile telephony and voice-controlled consumer electronics, the recorded speech signals are corrupted in various way by additive background noise, reverberation and far-end echo signals. This is mainly due to the fact that the recording microphone array is located at a certain distance from the speaker, which allows the microphones to record the noise and echo sources too. Additive background noise typically arises from computer fans, engine noise, audio equipment or other speakers present. It can originate from a localized noise source or be diffuse noise, coming from all directions. Reverberation is caused by reflections on the room walls and on other surfaces, such that the recorded signal consists of a direct path signal and multiple delayed and attenuated versions of it.

Depending on the acoustic environment, background noise and reverberation have a significant impact on speech communication quality. In noisy and reverberate rooms the intelligibility of the recorded speech drops considerably. In order to improve speech intelligibility and enhance the performance, the sound emitted by the speaker has to be recovered from the microphone recordings as ‘clean' as possible (i.e. reduce noise and reverberation).

Beamforming techniques are well-known techniques for noise suppression and dereverberation. In beamforming the different microphone signals are filtered and combined in such a way that the direction of the desired speech source is enhanced and the directions of the undesired noise sources are suppressed. Since the desired speaker is allowed to move around and the acoustic situation changes, adaptive filtering techniques are required to handle this time-varying acoustic environment.

1. INTRODUCTION

1.3 Principle of Beamforming

Beamforming is a technique used to identify the source (or sources) of signals. Using multiple sensors (i.e. microphones) arranged in a grid, it is possible using beamforming techniques to tell the directions from which signals are coming from.
The response of a single element is plotted on a polar graph in Figure 1.4 and 1.5, where the angle is offset from the beam directions, and the radius is the magnitude response (dB) in that direction. Element responses, determined generally by means of the 3 dB down point, are very wide - in this instance the width is about 90°.

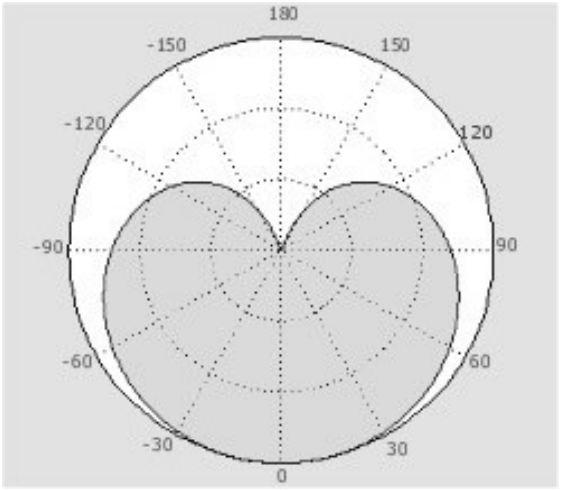


Figure 1.4 Microphone Signal [2]

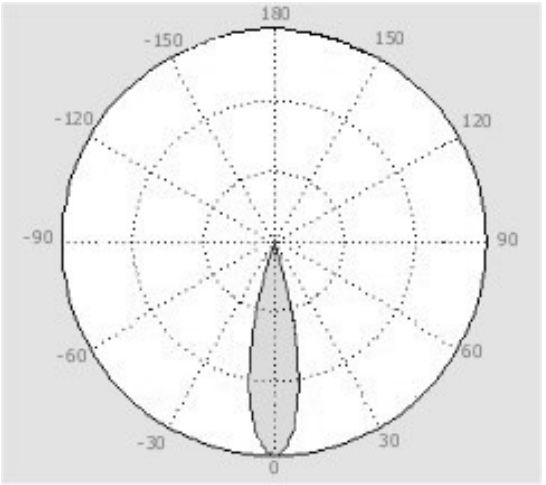


Figure 1.5 Beamformed Signal [2]

The goal of conventional beamforming is thus to delay and sum the outputs from the individual sensors in the array so as to increase the Signal to Noise Ratio (SNR) and in so doing to achieve a narrower response in a desired direction or set of directions. The pointing direction is referred to as the Maximum Response Axis (MRA) and can be chosen arbitrarily for the beams. In this way, when a source is detected in a given beam or sector of beams, the approximate direction where it comes from is known." [2]

1. INTRODUCTION

The simplest type of beamforming uses the "delay and sum" concept which is used in this project. Each microphone's signal can be delayed by an amount proportional to the distance between a known target and a microphone. Then all of these delayed signals are added together, resulting in a large signal component. As long as the noise is not coming from the exact same position as the desired signal, the noise signals will not be coherent and thus will not add up. The total noise power will remain approximately the same as for one microphone, but the total signal power will be multiplied by the number of microphones in the array.

The subsequent Figure 1.6 shows the delay and sum beamformer:

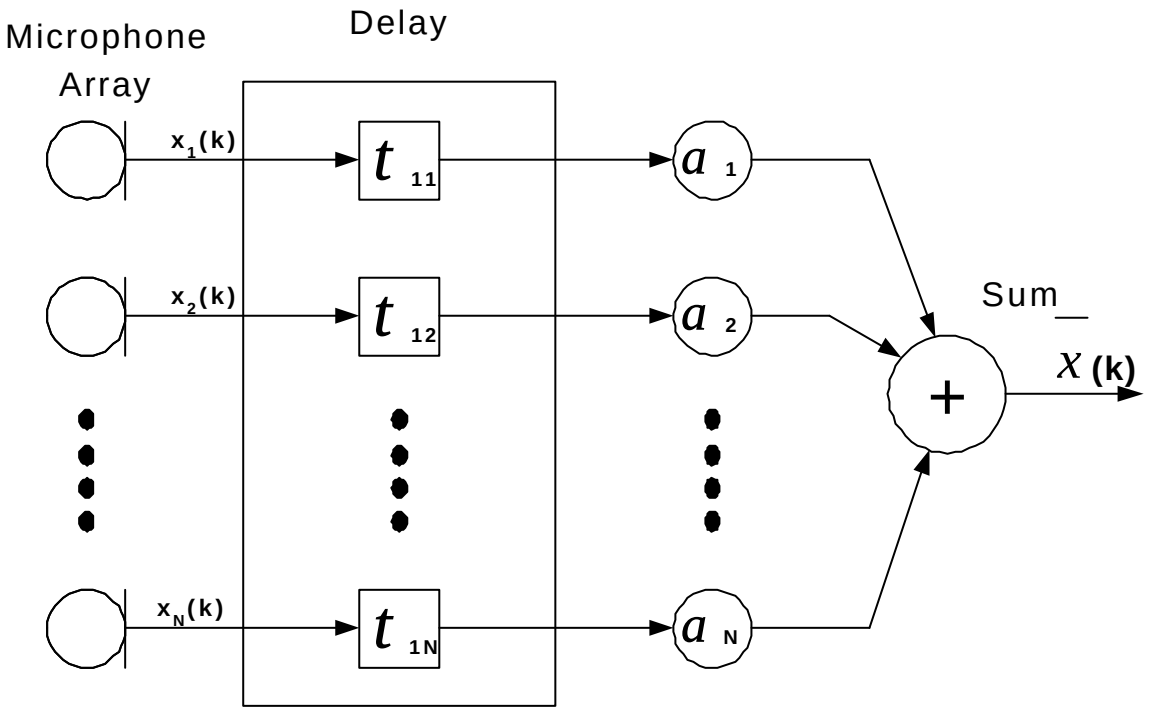


Figure 1.6 Delay and Sum Beamformer [4]

2. MICROPHONES

2.1 General Overview

"Microphones are used to convert acoustical energy into electrical energy. The microphone serves as an example of the idea that a specific purpose can be accomplished using many different physical principles.

Carbon:

Carbon microphones are made by encasing lightly packed carbon granules in an enclosure. Electrical contacts are placed on opposite sides of the enclosure. When an acoustical pressure is extorted on the carbon granules, the granules are pressed closer together which decreases the measured resistance. This is a very low quality acoustic transducer, but has been used in telephone handsets even through the current day.

Capacitor (condenser):

Capacitor microphones are made by forming a capacitor between a stationary metal plate, and a light metallic diaphragm. When an acoustical pressure impinges on the diaphragm, the diaphragm moves and causes the distance between it and the stationary plate to change. This will change the capacitance of the device. In order to measure the capacitance, one must apply a charge to the device. When this is done, the change in capacitance will result in a change in the voltage measured across the device.

Electret and Piezoelectric:

Electret microphones are capacitor microphones which use an electret material between the plates of the capacitor. Electrets are materials with a permanent polarization, and hence surface charge. A benefit to using electret microphones is that they do not need any external circuitry to create the charge, and hence are much easier to use. Many high quality, low cost electret microphones are available currently.

2. MICROPHONES

Piezoelectric crystals are crystalline structures which are similar to electrets in that they exhibit a permanent polarization of the individual cells. It is possible to use piezo sensors as microphones as well. Since they are in the form of a thin film, they are very useful if one is interested in detecting surface vibrations of an object.

Magnetic (moving coil):

Moving coil, or dynamic microphones are based upon the principle of magnetic induction. When an electrical conductor is moved through an electric field, a voltage is produced. This voltage is proportional to the velocity of the conductor. A moving coil microphone is made by attaching a coil of wire to a light diaphragm which moves in response to acoustical pressure. The coil of wire is immersed in a magnetic field, hence the movement of the coil in the magnetic field will create a voltage which is proportional to the acoustical pressure." [3]

2.1.1 Computer Desktop Microphone

Four computer desktop microphones pick up a speaker's voice. These microphones can be especially used for audio input like multi media applications. The subsequent listing shows the characteristics of the microphone:

- Electret microphone
- Omni-directional (pick up sound from all directions)
- Sensitivity: -67dB/ì Bar
- Microphone power source voltage: 1.5 Volt DC
- Impedance: 2000 Ù
- Frequency response: 100-16000 Hz

2. MICROPHONES

2.2 Microphone Arrays

- "*Linear Microphone Arrays (one dimensional)*: The linear arrays are very common in which the microphones are placed in a horizontal line. In particular, with a small amount of microphones an equal distance between each microphone is used. Usually, for a bigger amount of microphones a linear array will be used which includes several sub-arrays. Those sub-arrays are equidistant between each microphone as well and are working in different frequency ranges. In order that the microphones can be individually used several times, the sub-arrays have to be constructed the way that the microphone distance is always a multiple of the shortest microphone distance.
  Other theories propose to use non-equidistant microphones. The distances increase equally from the center microphone to both sides.

- *Two Dimensional Arrays:* In addition to the linear microphone arrays also the two dimensional arrays has to be mentioned. They will be placed vertically in front of the speaker. Some theories are using arrays where the microphones are placed equidistantly all over the area of a rectangle. But those rectangle arrays are not suitable for many practical applications like hands-free sets in cars.
  Two dimensional microphone arrays are very usual in which the microphones are mounted to each corner of a square. So that it is possible to place more microphones on this square array without enlarging its size, microphones can be installed equidistantly between each corner microphone.
  Finally the three dimensional arrays should be also mentioned. They will be used to detect the exact location of a speaker or for multiple beamforming." [4]

  The next figures show some opportunities for different types of microphones arrays:

2. MICROPHONES

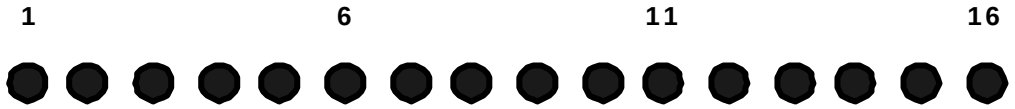


Figure 2.1 Linear Microphone Array [4]

Figure 2.2 Parallel Microphone Array [4]

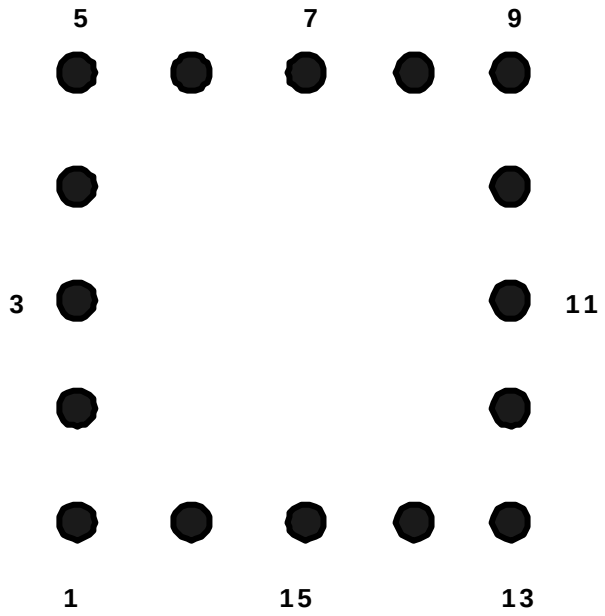


Figure 2.3 Square Microphone Array [4]

All arrays above contain 16 microphones which are placed in different ways but can be also used for a smaller amount of microphones like in this project. This board provides four audio channels thus the following mechanical construction was developed for only a four microphone array.

2. MICROPHONES

2.3 Mechanical Construction

The microphone array construction, Figure 2.4, is a linear microphone array with four microphones. The ground plate, in which a rail is mounted is made of wood. The four right angled microphone retainers will be pushed from the bottom up to the both edges

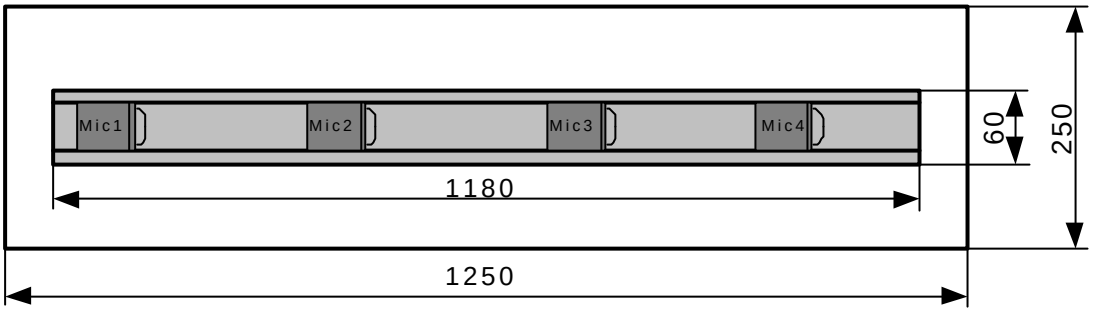


Figure 2.4 Top View of the Microphone Construction

of the rail by a spring. The microphone retainer is shown in Figure 2.5:

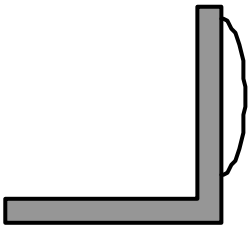


Figure 2.5 Side View of the Microphone Retainer

On each retainer's right side there is a computer desktop microphone base fixed by a double sided tape. Each microphone can be moved in vertical and in horizontal direction by pushing down the spring below the microphone retainer.

The minimum and maximum distances between each microphone in the array are 6.5 cm respectively 35 cm.

3. POWER SUPPLY

The power supply of the Printed Circuit Board (PCB) offers four different voltages which are supplied by the voltage regulators 7812, 7805 and 7905 and the DC-DC inverter MAX765.
The input of the power supply socket can be connected from 12 V to 15 V. It will be transformed by the voltage regulators and the DC-DC inverter to constant voltages of -5 V, +5 V , -12 V and +12 V. The capacitors in front and behind the voltage regulators are used to keep the output voltage stable.

The voltage regulator 7812 is shown as an example of the other voltage regulators in Figure 3.1 below:

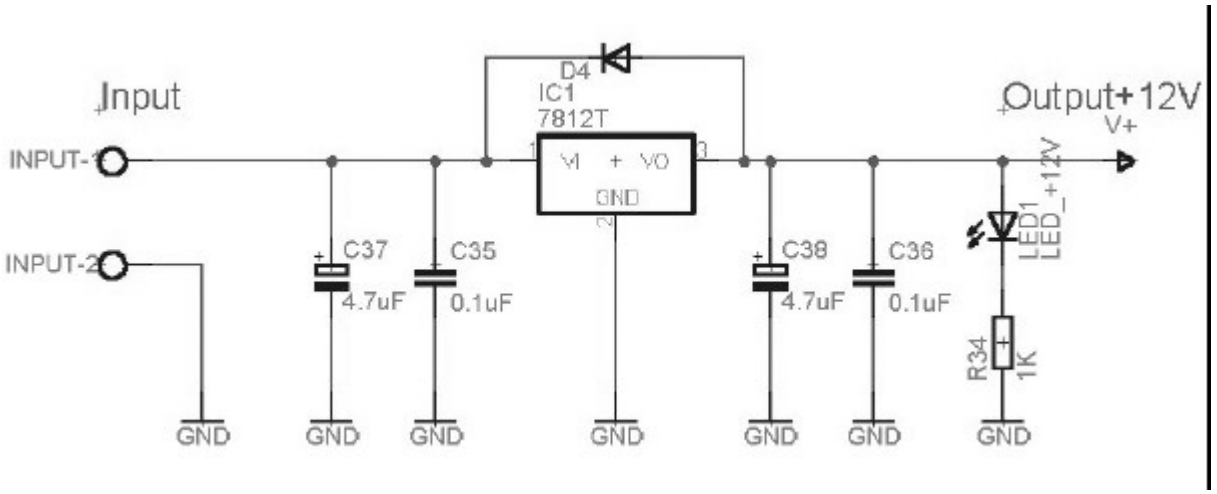


Figure 3.1 Voltage Regulators

The DC-DC inverter MAX765 accepts an input voltage range of 3 V to 8 V and provides a fixed output voltage of -12 V. In the configuration below ,Figure 3.2, the IC is powered by the differential voltage between the input (V+) and output (Out). The range of input and output voltages is limited to a 21 V absolute maximum differential voltage.

3. POWER SUPPLY

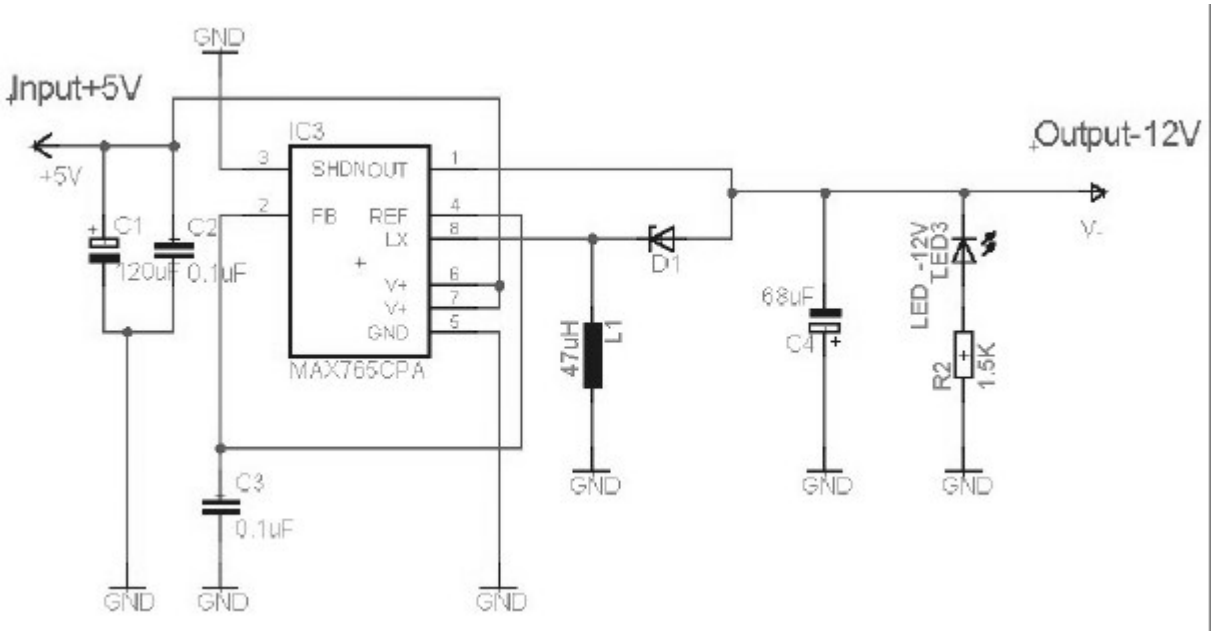


Figure 3.2 Power Supply MAX 765

"The MAX765´s high switching frequency demands a high-speed rectifier. Because of that a Schottky diode (D1) with a 0.75 A average current rating should be used, such as the 1N5817 or 1N5818 diode.

The value of the inductor (L1) should be within the range of 22 µH to 68 µH. If the inductor value is too low, the current in the coil will ramp up to a high level before the current-limit comparator can turn off the switch. Thus wasting power and reducing efficiency. A coil with a low DC resistance, preferably under 100 mΩ, provides highest efficiency.

The primary criterion for selecting the output capacitor (C4), is low Effective Series Resistance (ESR). The product of the inductor-current variation and the output capacitor's ESR determines the amplitude of the high-frequency seen on the output voltage. For optimum performance a capacitor with at least 68 µH should be used, low-ESR, and a voltage rating of at least 20 V.

3. POWER SUPPLY

The input bypass capacitor (C1) reduces peak currents drawn from the voltage source. It also reduces the amount of noise at the voltage source caused by the switching action of the MAX765. As with the output filter capacitor, a low ESR capacitor is highly recommend. For output current up to 250 mA, a 100 µF to 120 µF capacitor with a voltage rating of at least 20 V in parallel with a 0.1 µF capacitor (C2) is adequate." [5]

The LED's (LED1, LED2, LED3, LED4) at the output of each voltage regulator and the DC-DC inverter indicate if the output is active. In the case the regulators or DC-DC inverter is broken the LED of the corresponding line would not be lighten.

The following equations show the calculation of the pre-resistors for each LED:

-5 V supply: (3.1)

$$R1 = \frac{V - Ud}{Id} = \frac{-5V - 1.7V}{10mA} = 670\Omega$$

5 V supply: (3.2)

$$R3 = \frac{V - Ud}{Id} = \frac{5V - 1.7V}{10mA} = 330\Omega$$

-12 V supply: (3.3)

$$R2 = \frac{V - Ud}{Id} = \frac{-12V - 1.7V}{10mA} = 1.37k\Omega$$

12 V supply: (3.4)

$$R34 = \frac{V - Ud}{Id} = \frac{12V - 1.7V}{10mA} = 1.03k\Omega$$

4. PRE - AMPLIFIER

The first idea has been to implement this pre-amplifier as a Voltage Controlled Amplifier (VCA). This means that the signal gain depends on the input signal. Lower signals gain more than higher signals. But this kind of pre-amplifier is not really necessary because the difference between lower and higher speech signals is not that big. Of course the input signal of the microphones depends on the distance between speaker and microphone, but the application for this project is limited for only small distances like a hands-free set for mobile phones.
As a result of this is to use a pre-amplifier with a fixed gain. The Operational Amplifier (OP-amp) is operated as a non-inverting amplifier.

The Figure 4.1 below shows the circuit diagram of the pre-amplifier:

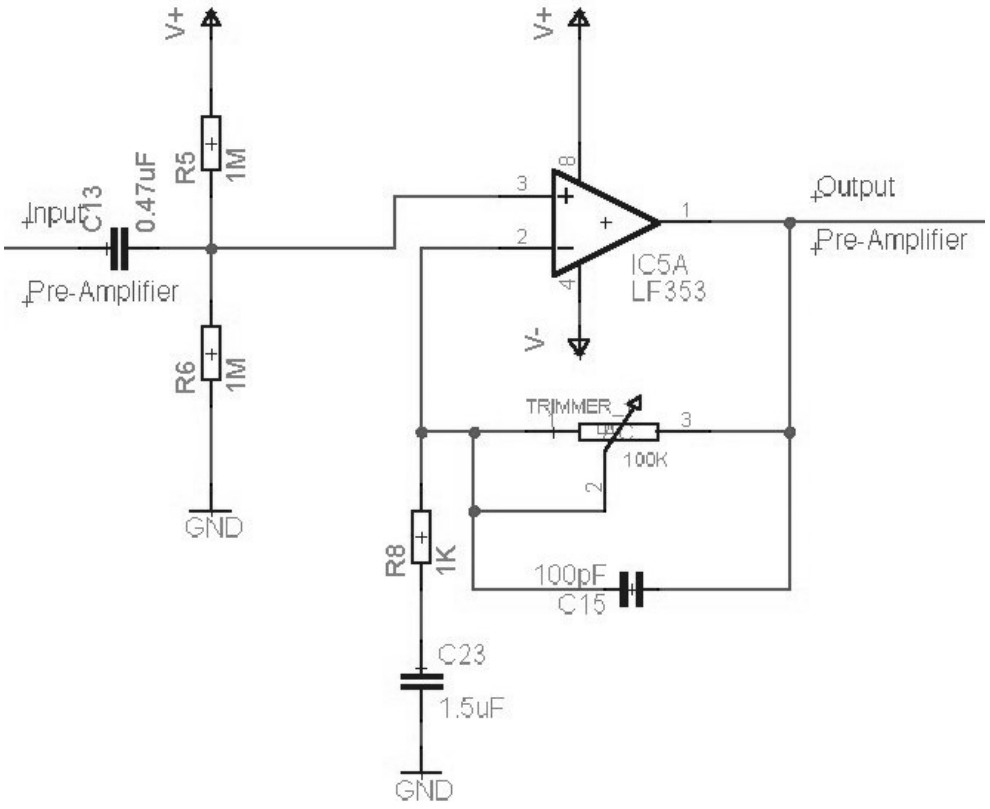


Figure 4.1 Pre - Amplifier Circuit Diagram

4. PRE - AMPLIFIER

The LF353 Integrated Circuit (IC) contains two integrated OP-amps. Each channel has an inverting and a non-inverting input and one output. The gain is adjustable with the ratio of two external resistors R8 and a trimmer. The trimmer has a range up to 100 kΩ, this means with the resistor R8 = 1 kΩ, the gain of this pre-amplifier is between 1 and 101.

At the input is a CR highpass filter (C13, R6) which separates the signal from possible Direct Current (DC). The cutoff frequency f_c is defined by :

$$f_c = \frac{1}{2*\pi*R6*C1} = \frac{1}{2*\pi*1M\Omega*0.47mF} = 0.338Hz \qquad (4.1)$$

The device is operated as a non-inverting OP-amp and the gain is adjustable with the two resistors R8 and a trimmer. The gain g is defined by:

$$G = \frac{R8 + Trimmer}{R8} = 1 + \frac{Trimmer}{R8} \qquad (4.2)$$

As the A/D converter has a maximum input voltage of 5 V the maximum speech signal at the input of the A/D converter should have a voltage range like demanded.

The experiment to adjust the pre-amplifiers gain is mentioned in chapter 9.

5. FILTER

Basically you can separate the filters into two categories. There are analog / digital and active / passive filters.
Both categories have the same basic types of filters:

- *Lowpass Filter:* Low frequency signals go through and high frequency signals are blocked
- *Highpass Filter:* High frequency signals go through and low frequency signals are blocked
- *Bandpass Filter:* Frequencies out of a specified range are blocked
- *Bandstop Filter:* Frequencies within a specified range are blocked

In this project lowpass filters and bandpass filters are only used. The lowpass filters are used for anti-aliasing and reconstruction filters.

5.1 Lowpass Filter - Anti-Aliasing Filter

“When selecting a filter, the goal is to provide a cutoff frequency that removes unwanted signals from the A/D converter input. Or at least attenuates them to the point that they will not adversely affect the circuit. An anti-aliasing filter is a lowpass filter that accomplishes this. The key parameters that need observation are the amount of attenuation (or ripple) in the pass band, the desired filter rolloff in the stop band, the steepness in the transition region and the phase relationship of the different frequencies as they pass through the filter.
The four basic filter types of active filters are:

- *Butterworth Filter*
- *Bessel Filter*
- *Chebychev Filter*
- *Elliptic Filter*

5. FILTER

The *Butterworth Filter* has the flattest pass band region, meaning it has the least attenuation over the desired frequency range.
The *Bessel Filter* has a more gradual roll-off but its key advantage is that it has a linear phase response. It means each frequency component is delayed by an equal amount of time as it passes through the filter. A linear phase response is often specified as a constant group delay, since group delay is defined as the derivative of the phase response with a respect to frequency.
The *Chebychev Filter* has a steeper rolloff but more ripple in the pass band.
The *Elliptic Filter* has the steepest rolloff.

For a simple anti-aliasing filter, often a simple single-pole passive RC filter is acceptable. But in other cases an active filter (i.e. using an OP-amp) works well. One advantage of an active filter is that for multi-order filters. The operation of the filter is less sensitive to the values of the external components, in particular, the 'Q' value of the filter." [6]

In this application an 2^{nd} order active lowpass filter is used which is designed by a filter development software. This 2^{nd} order lowpass filter is sufficient enough because there should not be any frequency components higher than half of the sample frequency (F_S /2 = 125 kHz) of the used SC bandpass filter. The name of this software program is called *AktivFilter1.2* and is available as a freeware version.

5.1.1 AktivFilter1.2 - Software

This program is a freeware version to develop 1^{st} and 2^{nd} order active lowpass and highpass filters and is very easy to use. As the language of this program is in German the English expressions of each used pull-down menu is written in brackets behind the German expression.

5. FILTER

After starting the executable file push the pull-down menu "*neues Filter*" (new filter) and select between *Tiefpass mit Sallen-Key Struktur* (lowpass filter) or *Hochpass mit Sallen-Key Struktur* (highpass filter).
In both filter types the same window will open: there it is possible to define the values and the characteristics of the filter. The most necessary options are explained below:

- *Charakteristik* (characteristic): You can choose the basic types of active filters which is necessary for the application.
- *Widerstandswerte* (values of resistors) : You can select the Exx - Series, (e.g. E12, E24, etc.)
- *Ordnung* (order): Only 1. and 2. order filters can be chosen in this freeware version
- *Grenzfrequenz* (cutoff frequency): -3 dB of the frequency response
- *Operationsverstärker* (OP - Amplifier): only three OP – types can be chosen

After everything is done just push the OK button and the program will generate the filter. A new window opens and it includes the frequency response of the filter. Furthermore you can push the second pull-down menu "*Ergebnis"* (result). There you can select *Dimensionierung* (dimensions) which includes the values of each used device or *Schaltbild* (circuit diagram) which shows the circuit diagram.
The following Figure 5.1 shows the circuit diagram of the active 2nd order lowpass filter:

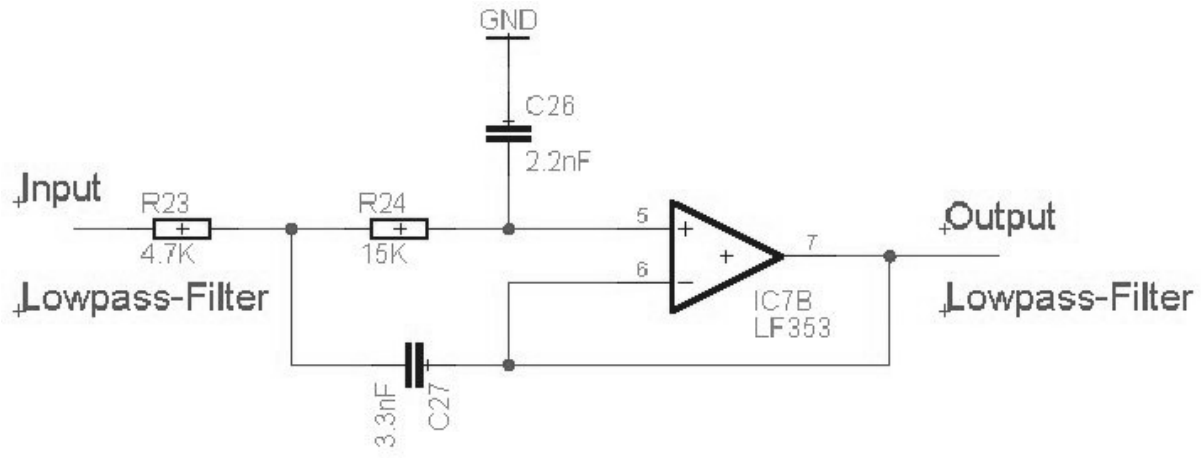


Figure 5.1 Circuit Diagram of the Active Lowpass Filter

5. FILTER

This 2nd order lowpass filter has "*Bessel*" characteristic and a "*Sallen-Key structure*". The cutoff frequency f_c is 5000 Hz.

The subsequent Table 5.1 shows the values of the used resistors and capacitors:

R1	R2	C1	C2	OP-Amplifier
4.7 kΩ	15 kΩ	2.2 nF	3.9 nF	LF358

Table 5.1 Values of Resistors and Capacitors

The following Figure 5.2 shows the frequency response of the 2nd order active lowpass filter:

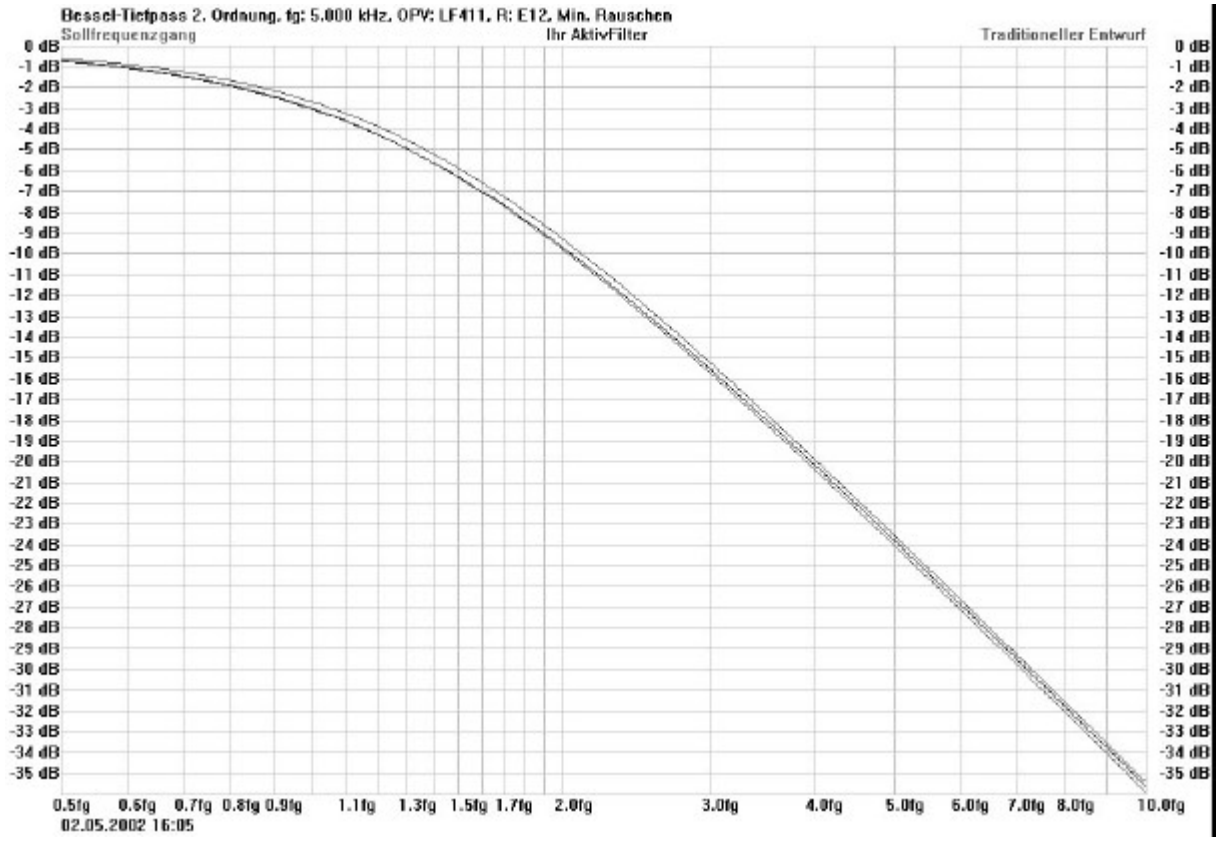


Figure 5.2 Frequency Response of 2nd Order Active Lowpass Filter

5. FILTER

5.2 Switched Capacitor (SC) Bandpass Filter

"Filters are very important in every sector of electronics. To build up a normal LC-Filter is usually very expensive. Thus more and more active filters are used in electronic circuits. Still many semiconductor companies offer also these Switched Capacitor (SC) filters which only need external resistors and no capacitors anymore. The filter frequency is defined by an external clock signal and is proportional to its frequency. The accuracy and the stability of these SC filters mainly depends on this external clock frequency.
It is also possible to cascade these filter ICs to get a higher order filter.
A disadvantage of these SC filters is that there can not be any frequency components higher than half of the sample frequency. This means it is necessary to use an analog lowpass filter in front of the SC filter input and sometimes even at the output. Because this filter generates a staircase signal and it includes high frequency components of the clock frequency." [7]

The first trial to implement a bandpass filter with switched capacitor devices has been with Maxim's MF10 SC filter.
"The MF10 is a dual 2^{nd} order, switched capacitor, state variable filter. Each of the two filter sections uses two switched capacitor integrators and an OP-amp to generate a second order function. The location on the poles is determined by the frequency of an external clock and 2 external resistors. No external capacitors are used. Fourth order filters can be made by cascading the two 2^{nd} order filter sections of the MF10, and higher order filters can be easily made by cascading more MF10s." [8]

The simplest circuit to implement a second order bandpass filter is *mode 1* or *mode 1a*. This minimum component count configuration uses only two or three external resistors.

5. FILTER

Design equations for *mode1a* with two resistors:

$$f_0 = \frac{f_{clk}}{100} or \frac{f_{clk}}{50} \quad (5.5)$$

$$Q = \frac{R3}{R2} \quad (5.6)$$

$$G = -\frac{R3}{R2} \quad (5.7)$$

f_0 = Center Frequency
f_{clk} = External Clock Frequency
Q = Quality Factor
G = Gain

Design equations for *mode 1* with three resistors:

$$f_0 = \frac{f_{clk}}{100} or \frac{f_{clk}}{50} \quad (5.5)$$

$$Q = \frac{R3}{R2} \quad (5.6)$$

$$G = -\frac{R3}{R1} \quad (5.8)$$

As the Center Frequency (f_0) is defined as 2.5 kHz and the ratio between the clock frequency and the Center Frequency (f_0) is adjusted to 50. The External Clock Frequency (f_{clk}) has to be 125 kHz. In order that the ratio is 50, pin 12 has to be connected to the supply voltage.

The Quality Factor (Q) is also defined by the following equation:

$$Q = \frac{f_0}{f_H - f_L} \quad (5.9)$$

f_H = Higher Cutoff Frequency
f_L = Lower Cutoff Frequency

The Higher Cutoff Frequency (f_H) is chosen as 5 kHz and the Lower Cutoff Frequency (f_L) is chosen as 300 Hz. As a result of this definition the factor Q is 0.532.

5. FILTER

With Q = 0.532 and a selected value of the resistor R2, typically between 10 kΩ and 100 kΩ, the other resistor R3 can be calculated by equation (5.6).

$$R3 = R2 * Q = 10k\Omega * 0.532 = 5.32k\Omega \qquad (5.7)$$

The Gain (G) of the bandpass filter at f_0 depends on the two external resistors R1 and R3 for *mode 1*. For a gain factor of -1 the resistor R1 has to be the same value as the resistor R3. (R1 = R3 = 5.32 kΩ)

The Figure 5.3 below illustrates the circuit diagram of the MF10 4th order bandpass filter:

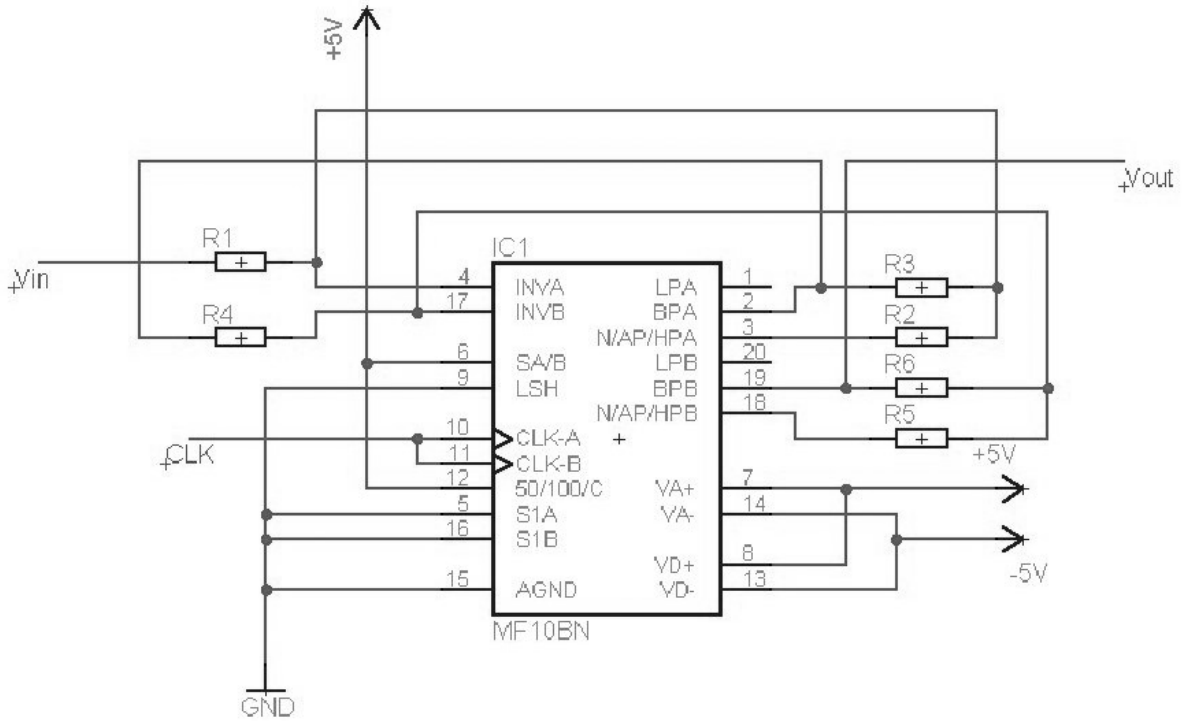


Figure 5.3 MF10 Circuit Diagram

5. FILTER

The signal comes in and goes through the resistor R1 to pin 4. The bandpass output of the first 2nd order section, pin 2, is connected to the second 2nd order section at pin 17 through another resistor R4.

This bandpass filter is just an alternative version for the following bandpass filter described in the next chapter below. As the MF10 ICs are not up to date anymore and in the case of higher order filters, at least two ICs are needed to get an 8th order filter. From this point of view it is not possible to use two ICs for one bandpass filter. It would mean that eight ICs has to be used for four audio channels and the board should not be that big in its dimensions.

As a result of this, an IC - LTC1068 - of Linear Technology is used. This IC contains four 2nd order switched capacitor filter sections and an external clock tunes the center frequency of each 2nd order filter section. The LTC1068 products differ only in their clock-to-center-frequency ratio. The clock-to-center ration is set to 200:1, 100:1, 50:1 or 25:1. The circuit diagram is developed with a filter program which is described in the following chapter.

5. FILTER

5.2.1 FilterCAD - Software

FilterCAD is a freeware software of Linear Technology to create lowpass, highpass, bandpass and notch filters with their ICs.
The first step is to decide between *Quick Design* or *Enhanced Design. Enhanced Design* is more accurate to develop a filter circuit because there are plenty of features to create more detailed filters.

The design parameters of the bandpass filter are:

- Pass band ripple (PR): 0.0 dB
- Stop band attenuation (SA): 10.0 dB
- Center frequency (F0): 2.500 kHz
- Pass band width (PBW): 4.400 kHz
- Stop band width (SBW): 7.200 kHz

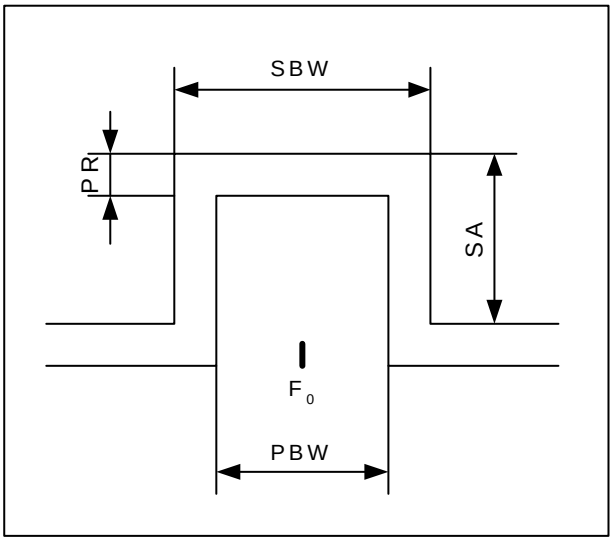


Figure 5.3 Filter Design

After each parameter is chosen the program generates the frequency response and the circuit diagram with the external resistors.

5. FILTER

But the resistor values are not normalized to the E12 - series. That means it is necessary to change the values by hand.

The subsequent Figure 5.4 shows the circuit diagram of the LTC1068 SC bandpass filter, developed by *FilterCAD* software:

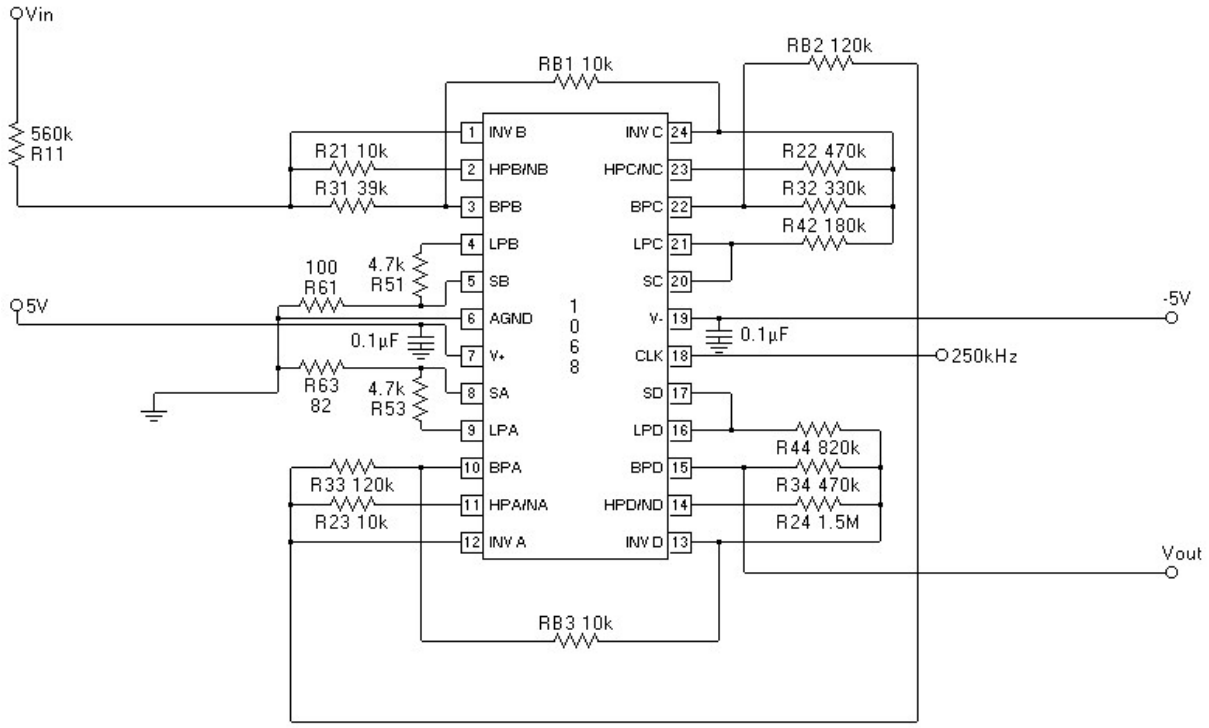


Figure 5.4 Circuit Diagram of LTC1068 SC Bandpass Filter

The signal comes in into the first stage of this four 2nd filter sections at Vin. After that the output of the bandpass filter of each section is connected with the input of the following section. At pin 15 is the output signal available.

As the center frequency of this 8th order bandpass filter is 2.5 kHz, the external clock frequency has to be 250 kHz. The clock-to-center frequency ratio is adjusted to 100:1. This LTC1068 IC is operable with single power supply (+ 5 V) or dual power supply (± 5 V).

5. FILTER

In previous experiments with this bandpass filter and a test board, problems appeared when the IC is operated with a single voltage supply. In this kind of operation a lot of distortion appears and no clear operation is guaranteed. For that reason the LTC1068 should be driven by a dual power supply (± 5 V).

The next Figure 5.5 shows the frequency response of the 8th order Bandpass Filter:

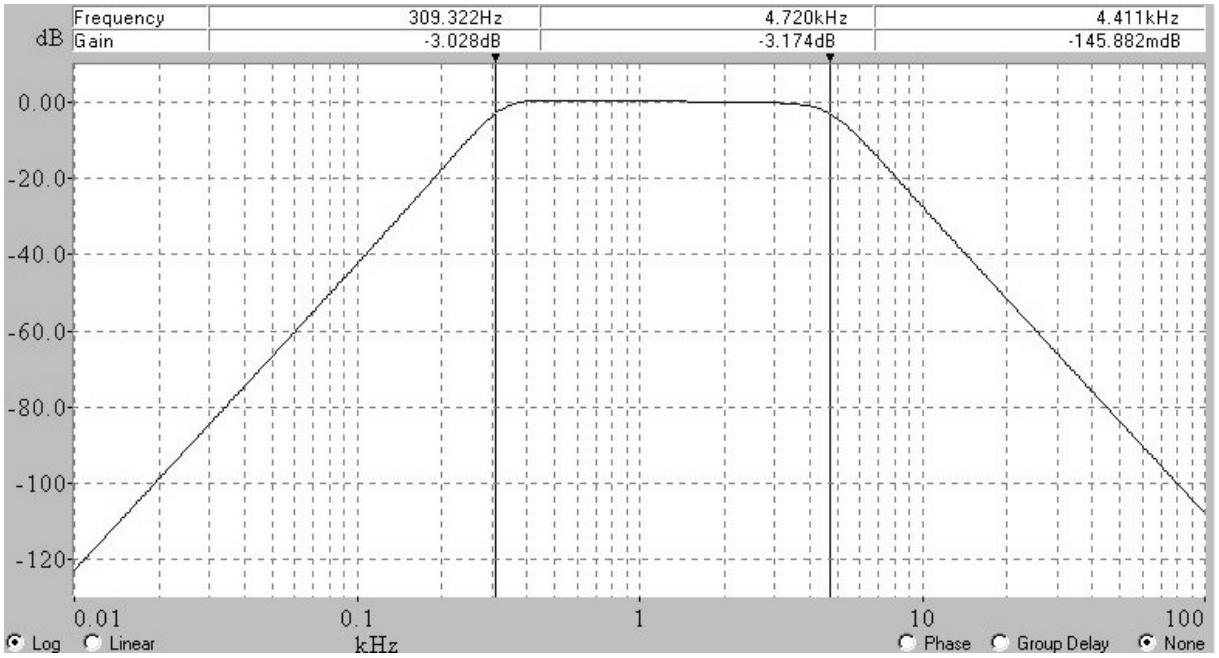


Figure 5.5 Frequency Response of 8th Order Bandpass Filter

In the diagram above, the cutoff frequencies of the bandpass filter are adjusted as demanded for the application of speech.
The lower cutoff frequency is about 300 Hz and the higher is about 4700 Hz and the steepness is -80 dB per decade. The gain in the pass band range is linear and always 0 dB.

5. FILTER

5.3 Clock Generator

"The clock generator to determine the center frequency of the SC filter is built up with the 14 stage binary counter 74HC4060 and is operated by a 16 MHz crystal. From the outputs Q4 to Q14 the different frequencies are available in the range of 967 Hz to 1 MHz. With a ratio of 100:1 of the SC bandpass filters the center frequencies are from 9.766 Hz up to 10 kHz." [9]

The following Table 5.2 shows the clock and center frequencies:

Output	Clock Frequency	Center Frequency
Q14	976.6 Hz	9.766 Hz
Q13	1.953 kHz	19.53 Hz
Q12	3.906 kHz	39.06 Hz
Q10	15.63 kHz	78.13 Hz
Q9	31.25 kHz	312.5 Hz
Q8	62.50 kHz	625.0 Hz
Q7	125.0 kHz	1.250 kHz
Q6	250.0 kHz	2.500 kHz
Q5	500.0 kHz	5.00 kHz
Q4	1000.0 kHz	10.00 kHz

Table 5.2 Center Frequencies [9]

This means the output Q6 of the 14 stage binary counter 74HC4060 is connected to the clock input of each SC bandpass filter.

It is also possible to connect an external clock generator to the board instead of the explained clock generator above. For this reason a jumper (JP1) is used to choose between external clock or internal clock.

5. FILTER

The subsequent circuit diagram in Figure 5.6 shows the clock generator:

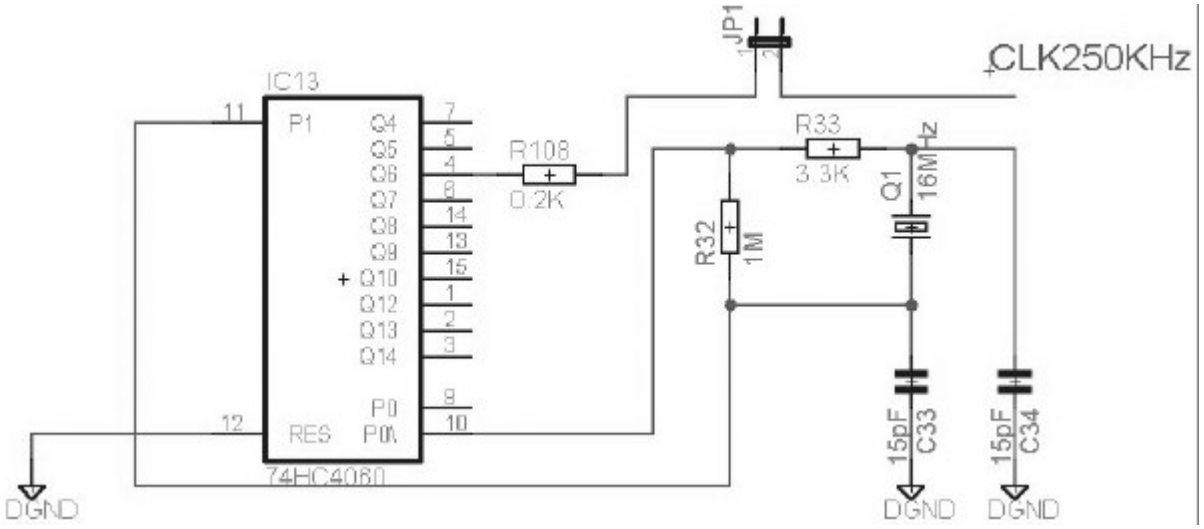


Figure 5.6 Clock Generator

5.4 Reconstruction Filter

This filter smoothes out the steps and reconstructs an equivalent analog signal based on the step levels of the DAC. As the output of the DAC is still a staircase signal the reconstruction filter is necessary to remove the high frequency components from the signal.

The reconstruction filter is, as well as the anti-aliasing filter, an active 2nd order lowpass filter. This reconstruction filter has the same characteristics as the lowpass filter which is already mentioned in chapter 5.1.1.

6. A/D CONVERTER

6.1 General Description

The microphones receive a time domain signal which will be pre-processed through the analog parts. They are mentioned in chapter 3 to chapter 5. The Analog-Digital-Converter (ADC) converts this signal into a discrete signal with a finite range of values. The two most important factors are the sampling rate or frequency and the resolution of the ADC.
The sampling frequency Fs has to be in conformance with *Shannon's sampling theory*. This means that the sampling frequency Fs should be twice the size of the highest frequency of the acoustic signal.

Shannon's sampling theory: $F_S = 2 * f$ (6.1)

For telecom applications a speech signal with a frequency range from 300 Hz to 3400 Hz is sufficient enough. The acoustic signal has to be sampled with 6800 Hz. The highest frequency of the SC bandpass filter is 4700 Hz thus the sampling frequency Fs has to be 9400 Hz.

The second factor is the resolution which indicates the size of each sample in bit. The more bits are used for the conversion of a sample the more accurate is the resolution of the time domain signal.
Although an 8 bit ADC should be sufficient enough to digitize a speech signal the low resolution causes an quantization error which appears as noise in the digitized signal. Therefore a resolution of 12 bit with 4096 quantization intervals is better to minimize such effects.

6. A/D CONVERTER

6.2 Analog-to-Digital Converter TLV2544

"The TLV2544 is a high performance, 12-bit low power, CMOS Analog-to-Digital Converter (ADC) which operates from a single 2.7 V to 5.5 V power supply. This device has three digital inputs, four analog inputs and a 3-state output. When interfaced with a DSP, a frame sync (FS) signal is used to indicate the start of a serial data frame.
In addition to a high-speed A/D converter and versatile control capability, these device has an on-chip analog multiplexer that can select any analog inputs or one of three internal self-test voltages. The sample-and-hold function is automatically started after the fourth SCLK edge (normal sampling) or can be controlled by a special pin, CSTART, to extend the sampling period (extended sampling). The normal sampling period can also be programmed as short (12 SCLKs) or as long (24 SCLKs) to accommodate faster SCLK operation popular among high-performance signal processors. Two different internal reference voltages are available and an optional external reference can also be used to achieve maximum flexibility." [10]

6.2.1 Input Scaling and Voltage Follower OP Amplifier

It should be noted that for V_{dd} = 5 V there is a 2.5 V DC offset voltage. It is produced by the node voltage of the voltage dividers (R109 / R110) multiplied by the amplifier gain, at the input of all four channels. The offset is used to convert the bipolar input to a single-ended input needed by the ADC. It is assumed that the analog signal is free of DC offset therefore the input capacitors (C56) with 0.1 µA are used to block possible DC voltage. If the incoming signal would have a DC offset, then the ADC Minimum Reference Voltage (REFM) is typically adjusted to the same value as the input signal DC offset voltage. And the Positive Reference Voltage (REFP) is raised by the same amount.

6. A/D CONVERTER

The Figure 6.1 below shows the input scaling and voltage follower operational amplifier:

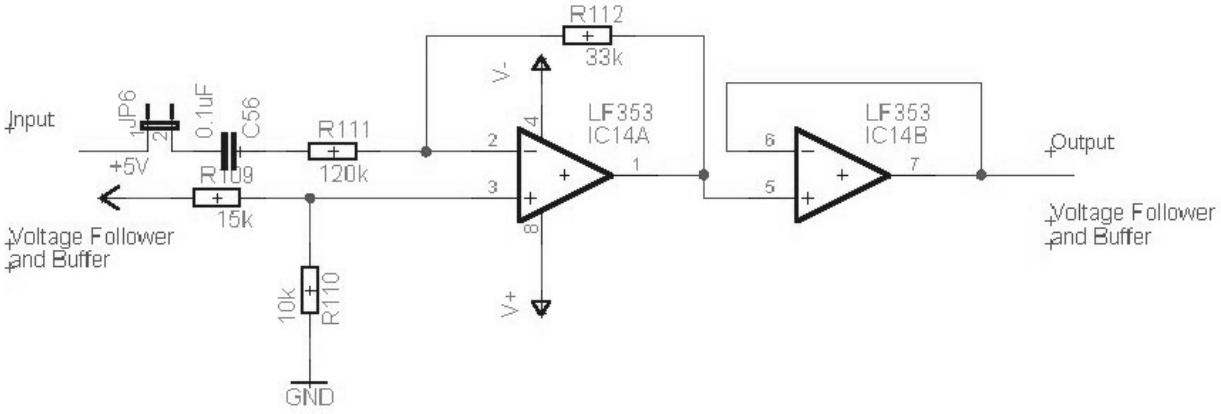


Figure 6.1 Voltage Follower and Buffer

6.2.2 Reference Voltage

The achievable accuracy for systems with Analog-to-Digital Converters (ADC) depends directly on the reference voltage applied to the ADC. Poor accuracy of the reference voltage degrades the overall system. For that reason a precision reference voltage is necessary such as the LM4120-5V which will be described in the subsequent pages.

As mentioned above the TLV2544 has also a built-in reference which is programmable to 2 V or 4 V. If the internal reference is used, REFP is set to 2 V or 4 V and REFM is set to 0 V.

In this application the reference is programmed as external. Thus, “the two reference input pins, REFP and REFM, can use an external reference voltage. The voltage level applies to these pins establish the upper and lower limits of the analog inputs to produce a full-scale and zero-scale reading respectively. The values of REFP, REFM and the analog input should not exceed the positive supply or be lower than GND

6. A/D CONVERTER

consistent with the specified maximum ratings. The digital output is full-scale when the input signal is equal to or higher than REFP and at zero when the input signal is equal or lower than REFM." [10]

The reference voltage is implemented by the LM4120-5V, "a precision micro power voltage reference, with up to 5 mA output current source, an output voltage of 5 V with a tolerance of ± 0.5 % and sink capability. The device operates with input voltages as low as 2 V up to 12 V consuming 160 µA supply current." [11]
The differential voltage between REFP and REFM should always be equal to or greater than 2.5 V for proper operation.

The following Figure 6.2 shows the LM4120 in application:

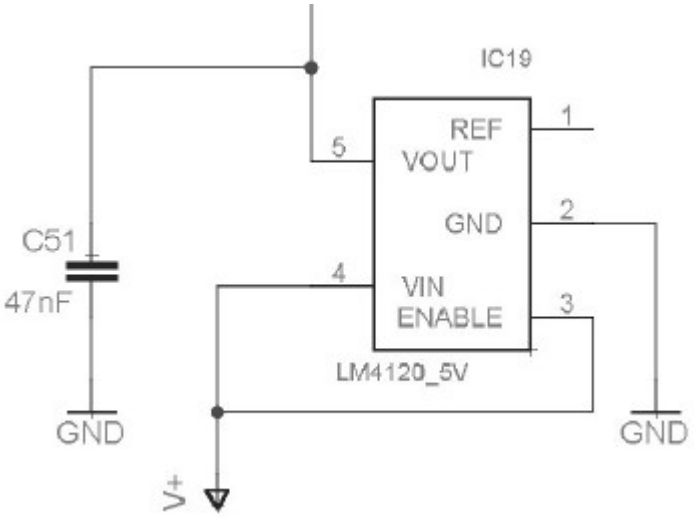


Figure 6.2 Reference Voltage 5 V with LM4120

"The circuit is designed to be stable with ceramic output capacitors (C51) in the range of 22 nF to 47 nF. An input capacitor is typically not required.
The reference pin is sensitive to noise and capacitive loading. Therefore, the PCB layout should isolate this pin as much as possible." [11]

6. A/D CONVERTER

6.3 Interfacing TLV2544 with TMS320C31

"Data transfer in normal operation consists of a DSP command for the ADC to start sample and convert. The ADC interrupts the DSP after a specified time, during which that sample and convert is completed, to notify the DSP that the data is ready to be read. Before all these processes can be performed, initialization and configuration are required for both devices to work properly. This application describes the standard serial port configuration for the TMS320C31 DSP which is used for interfacing of the ADC and microprocessor. The following sections describe how the DSP and the ADC are configured." [12]

Figure 6.3 shows the typical pin-to-pin connection interfacing between the DSP and the TLV2548 ADC:

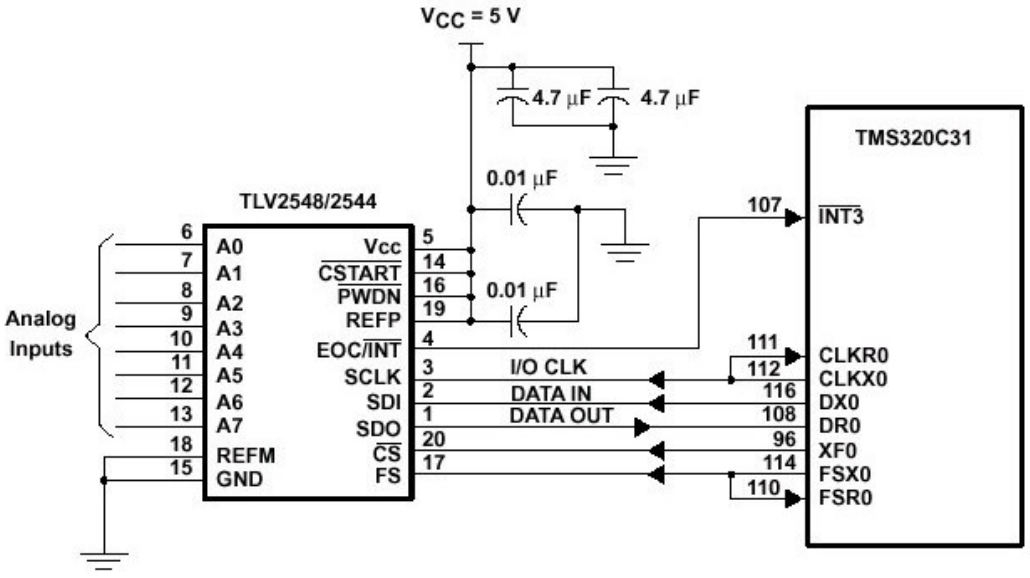


Figure 6.3 Interfacing TLV2544 with TMS320C31 [12]

"The regulated 5 V supply is applied to the ADC V_{CC} pin. A 4.7 µF capacitor keeps the entire circuit supply stable against any significant current changes during ADC operation.

6. A/D CONVERTER

The 0.01 μF (or 0.1 μF) bypass capacitor keeps the ADC supply, as well as the positive reference voltage, ripple-free.
The positive (REFP) and negative (REFM) reference voltages define the analog conversion range of the ADC and specify the maximum input signal level at the analog inputs, A0 to A3.

This glueless logic interface is described below:

- The DSP selects the ADC by asserting the CS pin of the ADC through the XF output of the DSP.
- The transmit clock output of the DSP, CLKX, provides a fixed data clock into the SCLK input of the ADC and into the receive clock, CLKR, of the DSP.
- The transmit frame-sync output, FSX, initializes every data transfer by sending a frame-sync pulse to the ADC FS input, as well as to the receive frame-sync input, FSR.
- The DSP initializes the ADC by transferring a 4-bit control word from the DX output into the SDI input of the ADC.
- After the conversion process is complete, the ADC generates an interrupt, EOC/INT, and provides it to the INT3 input of the DSP to initiate the DSP reading of the conversion data.
- The ADC clocks out the digital conversion result on the SDO pin, and into the DR input of the DSP.

The TMS320C31 DSP has one standard bi-directional serial port. The TMS320C31 serial port is a versatile communication channel that allows interfacing to most serial interface analog conversion chips without glue logic. The serial port can be configured to transfer 8, 16, 24, or 32 bits of data per word simultaneously in both directions. The clock for the serial port can be supplied externally, or can originate internally through the serial port timer and period registers.” [12]

6. A/D CONVERTER

"The serial port is used here to transmit and receive data between the DSP and the ADC, and the configuration described below is specific to the way that the DSP communicates with the ADC for this application. The DSP serial port requires a little more time and understanding to initialize and configure than the data converters. This report will explain the serial interface in some detail. Six control lines from the DSP are used to interface to the data converters:

CLKX *Transmit clock input or output*

This signal clocks data from the transmit shift register (XSR) to the data transmit (DX) pin. The serial port can be configured for internal clock generation or to accept an external clock. If the port is configured to generate the data clock on-chip, CLKX becomes an output, providing the data clock for the serial interface. If the port is configured to accept an external clock, CLKX becomes an input, receiving the external clock signal.

FSX *Transmit frame synchronization input or output*

FSX indicates the start of a data transfer. The serial port can be configured for internal frame-sync generation or to accept an external frame-sync signal. If the port is configured to generate the frame-sync pulse on-chip, FSX becomes an output. If the port is configured to accept an external frame-sync pulse, this pin becomes an input.

DX *Serial data transmit*

DX transmits the actual data from the transmit shift register (XSR).

CLKR *Receive clock input*

CLKR always receives an external clock for clocking the data from the data receive (DR) pin into the receive shift register (RSR).

6. A/D CONVERTER

FSR *Receive frame synchronization input*

FSR always receives an external frame-sync pulse to initiate the reception of data at the beginning of a frame.

DR *Serial data receive*

DR receives the actual data, which are clocked into the receive shift register (RSR).” [12]

The following Table 6.1 shows the pin-to-pin connection between TLV2544 ADC and TMS320C31 microprocessor:

TMS320C31	INT3	CLKR0	CLKX0	DX0	DR0	XF0	FSX0	FSR0
TLV 2544	INT	SCLK	SCLK	SDI	SDO	CS	FS	FS

Table 6.1 Pin-to-Pin Connection TLV2544 to TMS320C31

The TMS320C31 microprocessor is part of DSP Starter Kit which provides the mentioned pins as externally available pins on this DSP Starter Kit board. As the developed hardware has a single-row connector, both parts - ADC and microprocessor - can be easily connected by a flat ribbon cable.

7. D/A CONVERTER

7.1 General Description and D/A Converter TLV5619

After processing the speech signals, communication is again needed with the outside world. A Digital-to-Analog Converter (DAC) connects the digital world with the analog world. The processed signals of the TMS320C31 are transmitted to the DAC by the 12 parallel data pins from D0 to D11. Different output levels from the DAC are produced based on the digital word on its input. This step-level signal is passed through a lowpass output filter (reconstruction filter) which is explained in chapter 5.4.

The following Figure 7.1 shows the pin-to-pin connection between TMS320C31 and the 12 bit DAC TLV5619:

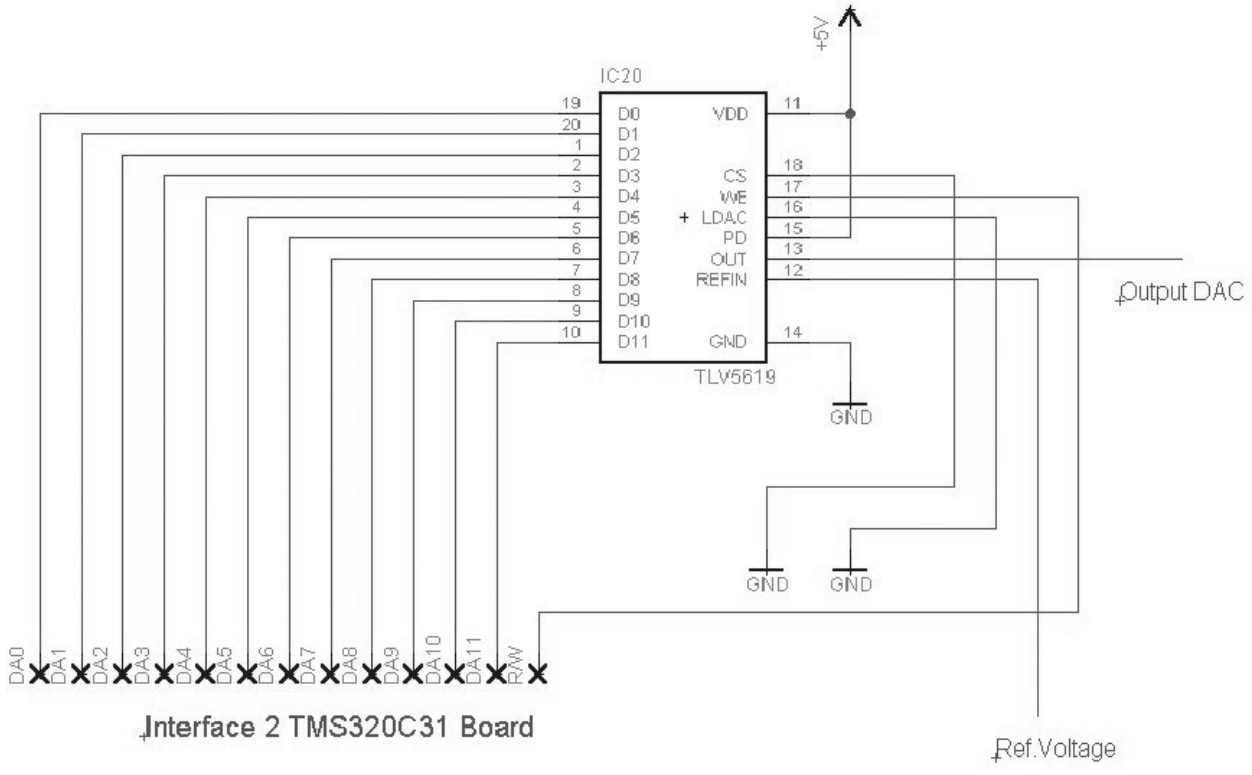


Figure 7.1 Pin-to-Pin Connection TMS320C31 to TLV5619

7. D/A CONVERTER

Interface 2 in Figure 7.1 is also a single-row connector with 13 pins. This connector is mounted on the developed hardware to interface the DAC with the microprocessor by a flat ribbon cable. The microprocessor's pins are also available on the DSP Starter Kit board as external pins.

Table 7.1 illustrates the pin-to-pin connection between TMS320C31 microprocessor and TLV5619 DAC:

TMS320C31	D0	D1	D2	D3	D4	D5	D6
TLV5619	DA0	DA1	DA2	DA3	DA4	DA5	DA6

TMS320C31	D7	D8	D9	D10	D11	R/W
TLV5619	DA7	DA8	DA9	DA10	DA11	WE

Table 7.1 Pin-to-Pin Connection TMS320C31 to TLV5619

The reference voltage of the DAC as well as the reference voltage of the ADC is responsible for the resolution and accuracy of the analog output signal. The voltage of this reference is limited to 2.048 V and is less than the reference voltage of the ADC.

The input level of the computer sound cards has almost the same maximum input voltage as the reference voltage of the DAC. Thus further experiments can be implemented to check the improved speech or audio signals.

8. PRINTED CIRCUIT BOARD (PCB) DEVELOPMENT

8.1 EAGLE Layout Editor

The Printed Circuit Board (PCB) of this diploma thesis is developed by the EAGLE Layout Editor program. The software contains a schematic editor, a layout editor and an auto router module.
Since not every IC is present in the main library of the program it is necessary to construct libraries for the following ICs:

- LTC1068 SC bandpass filter
- TLV2544 A/D converter
- LM4120 voltage reference
- TLV5619 D/A converter

Each library contains the symbol, the package and the device of each component. The packages of all ICs mentioned above are implemented as Surface Mounted Devices (SMD) except the LTC1068 SC bandpass filter. Its package is a conventional 24-Lead Plastic Dual-In-Line Package (PDIP).

When the schematic plan is created and all devices are placed in the layout editor the auto router module can be used to route the air wires on the board. As the auto router is not able to route all air wires on the board in complex layouts it is inevitable to route the remained air wires by hand.
The last phase is to apply the integrated Design Rule Check (DRC) of the program to check the design rules before the layout of the board is finished. The design rules check for example if the distances between wire and wire or wire and pad are big enough.

The following design rules are arising out of the datasheets [5], [11], [13] of some ICs which are used on the board.

8. PRINTED CIRCUIT BOARD (PCB) DEVELOPMENT

8.2 Layout Rules

- ***MAX765 DC-DC Inverter:***

    - C2 (Figure 3.2) must be placed as close as possible to V+ and GND pins.
    - Minimize ground noise by connecting GND, the input bypass capacitor ground lead and the output filter ground lead to a single point. (star ground configuration)

- ***LTC1068 SC bandpass filter:***

    - V+ and V- should be bypassed with a 0.1 µF capacitor to an adequate ground.
    - An analog ground surrounding the package is recommend.
    - The analog ground plane should be connected to any digital ground at a single point.
    - The power supply for the clock source should not be the filters power supply.
    - The clock signal should be routed from the right side of the IC package and perpendicular to it to avoid coupling to any input or output analog signal path.
    - In a printed circuit layout any signal trace, clock source trace or power supply trace should be at least 0.1 inches away from any inverting input pins.

- ***LM4120 voltage reference:***

    - To reduce the stress-related output voltage shifts, the reference should be mounted on the flow flex areas of the PCB such as near to the edge or the corner of the PCB.

8. PRINTED CIRCUIT BOARD (PCB) DEVELOPMENT

8.3 Version Update

Some modifications of the circuit diagrams and the layout of the PCB version 1 has to be done. The renewal of both is the updated version 2a which is enclosed in Appendix A and Appendix B. The following improvements are listed below:

- Sheet 1/6: Diode D2 is turned around
- Sheet 1/6: Capacitor C5 is turned around
- Sheet 2/6: Jumper J2 and J3 are inserted
- Sheet 3/6: Jumper J4 and J5 are inserted
- Sheet 5/6: Jumper J6 – J9 are inserted
- Sheet 6/6: OR-Gate NC7S32 is removed
- Sheet 6/6: Pin CS of DAC TLV5619 connected to GND
- Sheet 6/6: Pin LDAC of DAC TLV5619 connected to GND
- Sheet 6/6: Pin WE of DAC TLV5619 is connected to R/W of TMS320C31
- Layout board: Package LTC1068 is changed
- Layout board: Trimmer3 is turned around
- Layout board: Trimmer4 is turned around

Explanation:

- The jumpers J2 - J9 on the sheets 2/6, 3/6 and 5/6 are inserted to use the printed circuit board also without the SC bandpass filter.
- The improvements on sheet 6/6 are done because the interfacing between the DAC TLV5619 and TMS320C31 is also possible without an OR-gate. It is used in the older version 1. The following pins CS, LDAC and WE of the DAC TLV5619 are now connected to GND or direct to the TMS320C31 microprocessor without the OR-gate NC7S32.
- The pin distance of the LTC1068's package has been wrong and is changed.

9. EXPERIMENTS

Experiment 1: Adjustment of the trimmers respectively the gain of the pre-amplifiers

This experiment is executed to adjust the trimmers of each pre-amplifier respectively the gain. Thus the maximum input speech signal is adjusted to the reference voltage of the A/D converter.
A speech source says “one” with an average loudness and a distance of 30 cm to the microphone. This causes an output voltage of approximately 50 mV_p at the microphones output.
As the maximum reference voltage of the A/D converter is set as 5 V and the gain factor of the anti-aliasing filter and SC bandpass filter is 0 dB at the passband, the gain of the pre-amplifier has to be 50.

The subsequent Figure 9.1 shows the output speech signal of the microphone.

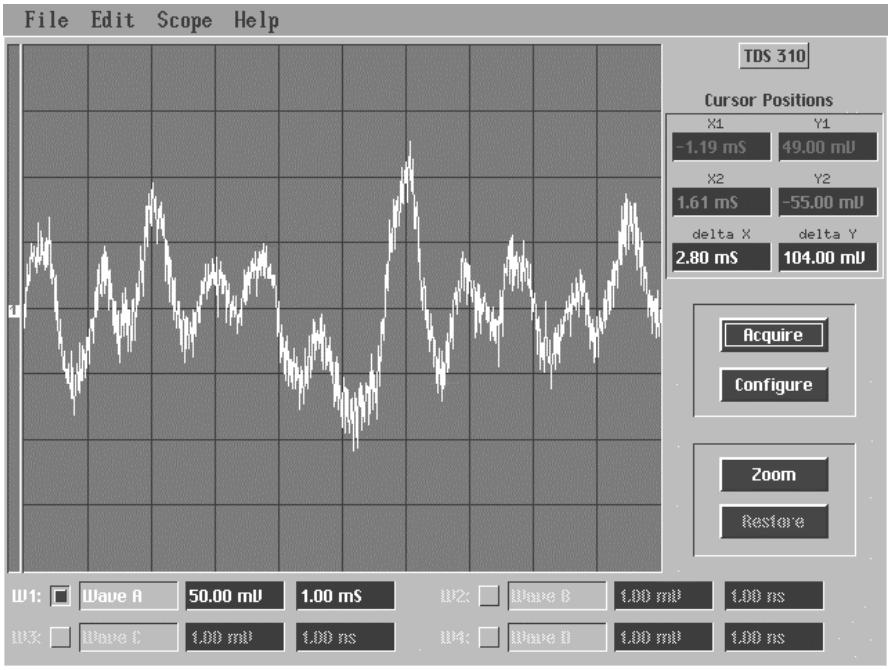


Figure 9.1 Speech Signal at the Microphone Output

9. EXPERIMENTS

This 50 mV_p microphone output voltage will be amplified to 2.5 V and is also added by 2.5 V DC of the input scaling circuit. Therefore the maximum of the reference voltage is reached and the A/D converter causes a full scale.
With equation (4.2) and a resistor R8 = 1 kΩ, the trimmer value is 49 kΩ.

As in Figure 9.1 is shown, the interference and the noise are proportionally big compared to the wanted signal.

Experiment 2: Measurement at the pre-amplifier's output

With the adjusted gain and the same conditions from *Experiment 1* the speech signal at the pre-amplifier's output is measured and shown in the following Figure 9.2:

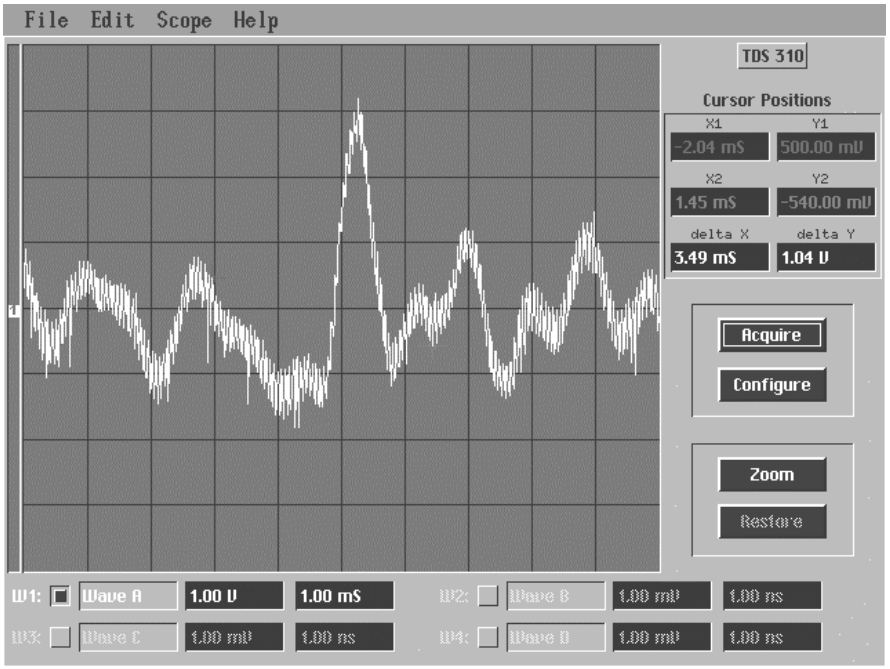


Figure 9.2 Speech Signal at Pre-Amplifier's Output

The signal is approximately 50 times bigger as the original input speech signal. This signal contains as well as the original signal (Figure 9.1) some noise and interference.

9. EXPERIMENTS

Experiment 3: Measurement at the anti-aliasing filter's output

The same measurement conditions are used as in the previous experiments above. A speech source says "one" with a distance of 30 cm to the microphone.

The signal at the anti-aliasing filter's output is shown in the following Figure 9.3:

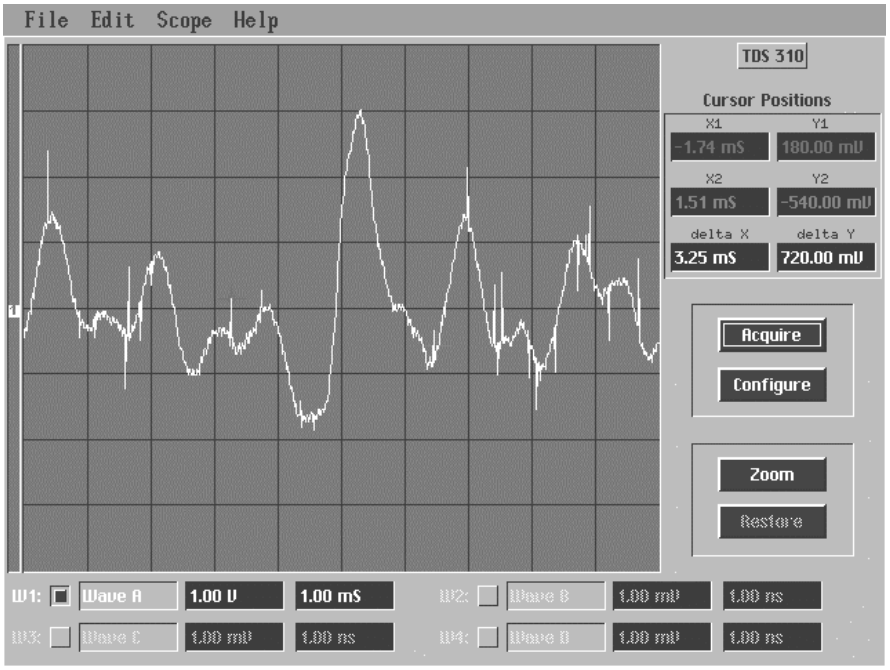


Figure 9.3 Speech Signal at Anti-Aliasing Filter's Output

This signal contains only a few interference peaks. The amplitudes of this signal are still approximately 2.5 V. As the anti-aliasing filter has a gain of 1 (0 dB) in the passband, the speech signal should not be different in its amplitude compared to the signal of the pre-amplifier's output.

9. EXPERIMENTS

Experiment 4: Measurement at the SC bandpass filter's output

The next Figure 9.4 illustrates the speech signal at the SC bandpass filter's output:

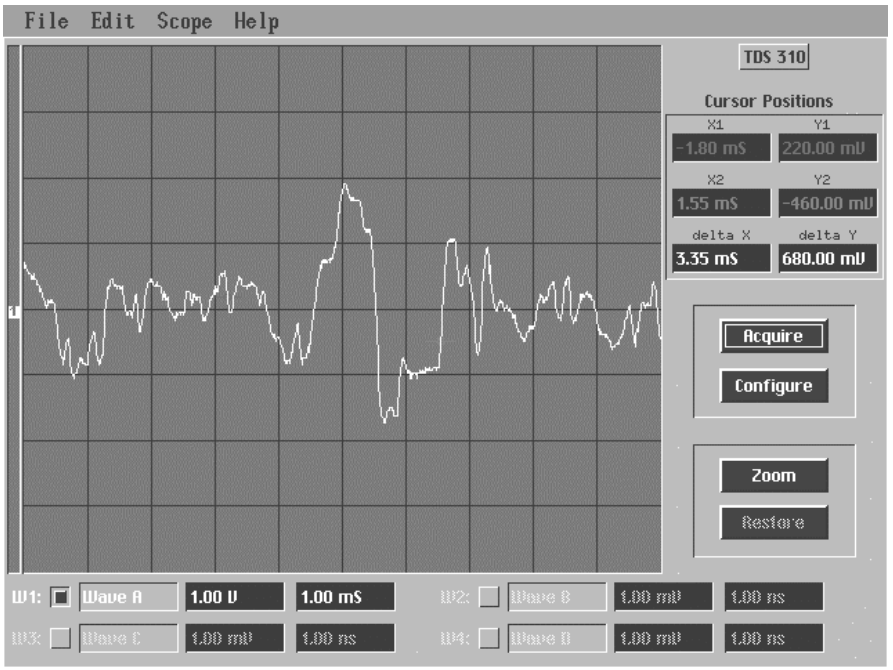


Figure 9.4 Speech Signal at SC Bandpass Filter's Output

The signal at the SC bandpass filter's output is almost free of any interference and noise. Only one little interference peak is visible in Figure 9.4. The amplitudes of the signal are almost the same as at the anti-aliasing filter's output because the gain in the passband of the SC bandpass filter is also 1 (0 dB).
Evidently there are some differences in the amplitudes because of the inequality of the speech source.

Further measurements could not be done with the ADC or DAC. The source codes to initialize the ADC and DAC which are part of another diploma thesis [1] are not finished at the time of the documentation.

10. CONCLUSIONS AND EXTENSIONS

10.1 Conclusions

The goal of this project is to develop a four channel board which processes speech signals and transfers them to the TMS320C31 microprocessor by a serial port interface.

The best solution could not be found for the different hardware parts. This is mostly because the used ICs and other components are restricted to only one electronic catalog which has a small range of products for this application.
Furthermore the SC bandpass filter LTC1068 caused a lot of problems. Not only during the experimental stage but even when the PCB is produced. For that reason the alternative SC bandpass filter MF10 is also mentioned in the documentation. This IC caused less problems than the other IC but it could not be used because the reasons mentioned in chapter 5.2.
Additionally, all four SC bandpass filters with their external components like resistors and capacitors take one third of the whole PCB. The original size of the PCB is shown in Appendix B.

From this point of view it would be better to build up a new audio processing board without an analog bandpass filter. This would reduce the size of the PCB enormously. A smaller size would mean that this project could be used better for a larger quantity of applications; such as hands-free mobile telephony in cars where space is a big problem.

To take all these arguments into consideration would mean that one should use a digital Finite Impulse Response (FIR) bandpass filter instead of an analog filter. This FIR filter and further hardware advisement will be shortly described in the following chapter.

10. CONCLUSIONS AND EXTENSIONS

10.2 Extensions

The best solution to minimize the size of the board but still have all the features mentioned in the last chapters is to use an analog interface chip such as TLV320AIC25 of Texas Instruments. This chip can be easily connected to many micro processors of Texas Instruments.
This IC provides four analog input channels and contains the same audio signal processing as this project. Except the bandpass filter which can be implemented as a digital FIR bandpass filter.

The subsequent Figure 10.1 shows the functional block diagram of one input channel:

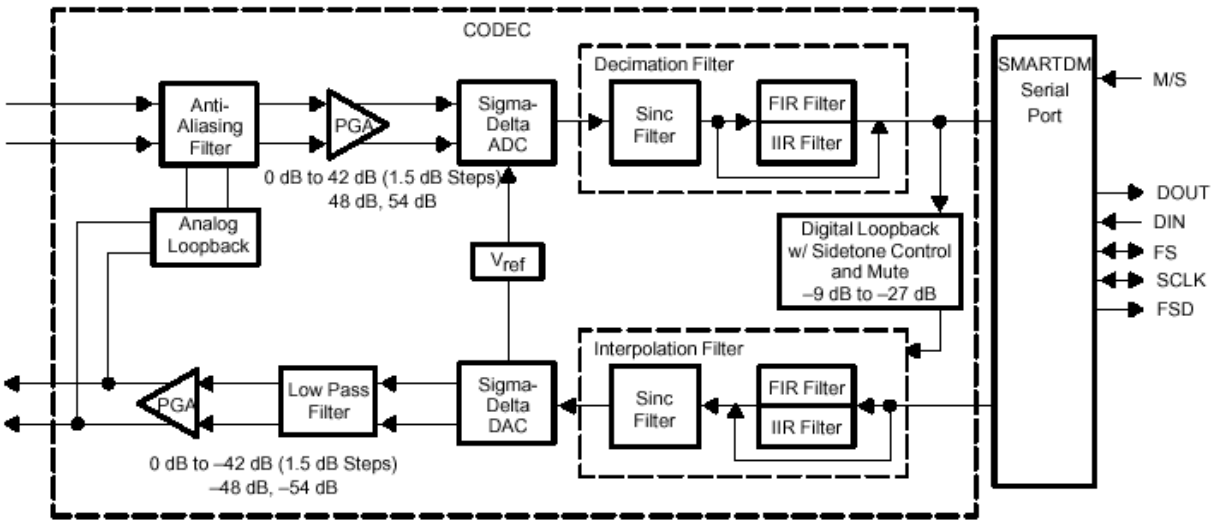


Figure 10.1 Functional Block Diagram of TLV320AIC25 [14]

The device features two 16-bit sigma-delta A/D converters, two 16-bit sigma-delta D/A converters and programmable sample rates up to 26 kHz. Furthermore there is an anti-aliasing filter, pre-amplifier and reconstruction filter included in one CMOS chip.

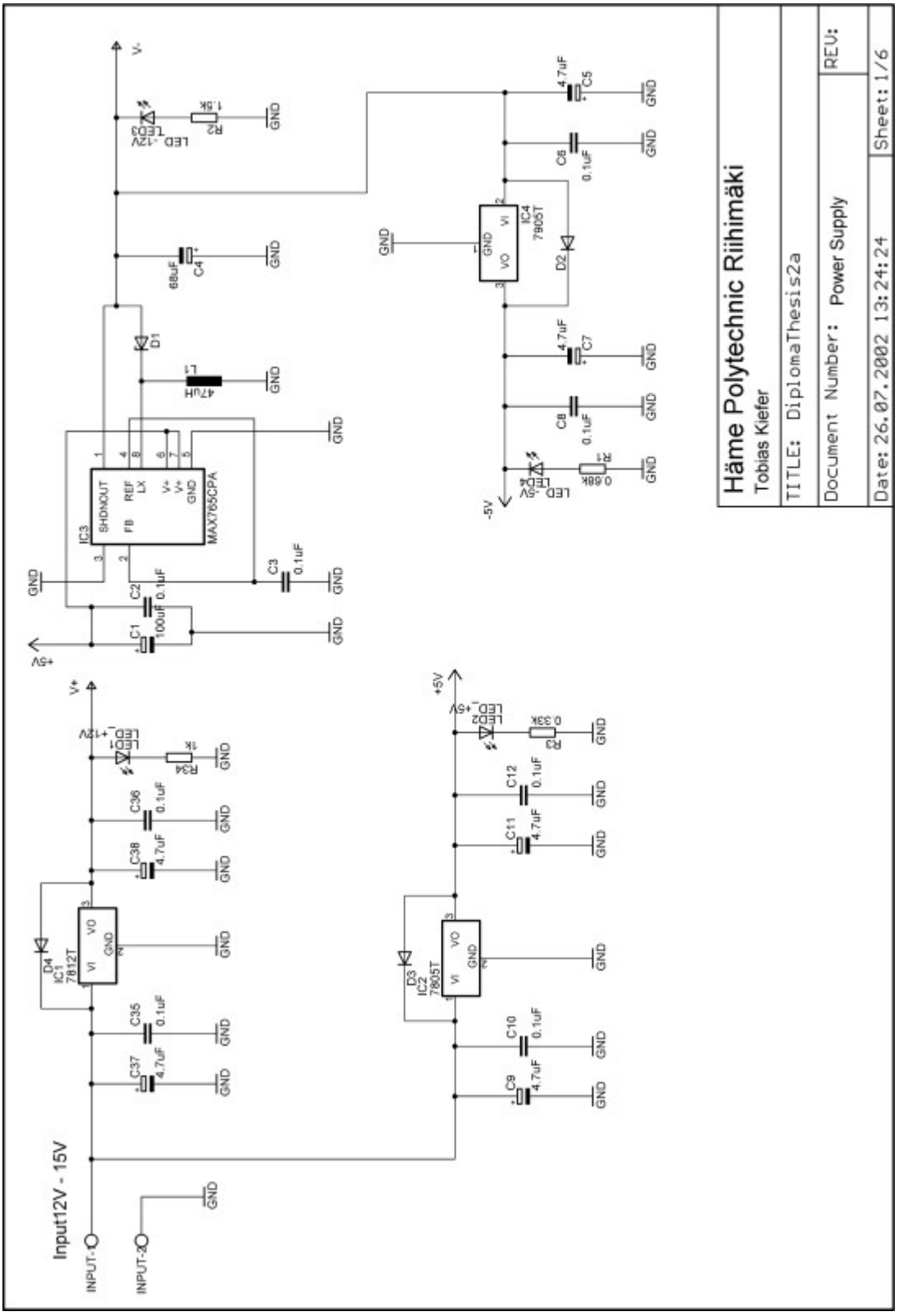
10. CONCLUSIONS AND EXTENSIONS

These features make the TLV320AIC25 ideal for digital telephony, Voice over IP (VoIP) phone and gateway, voice recognition, hands-free set and other applications utilizing low-power voice digitization.

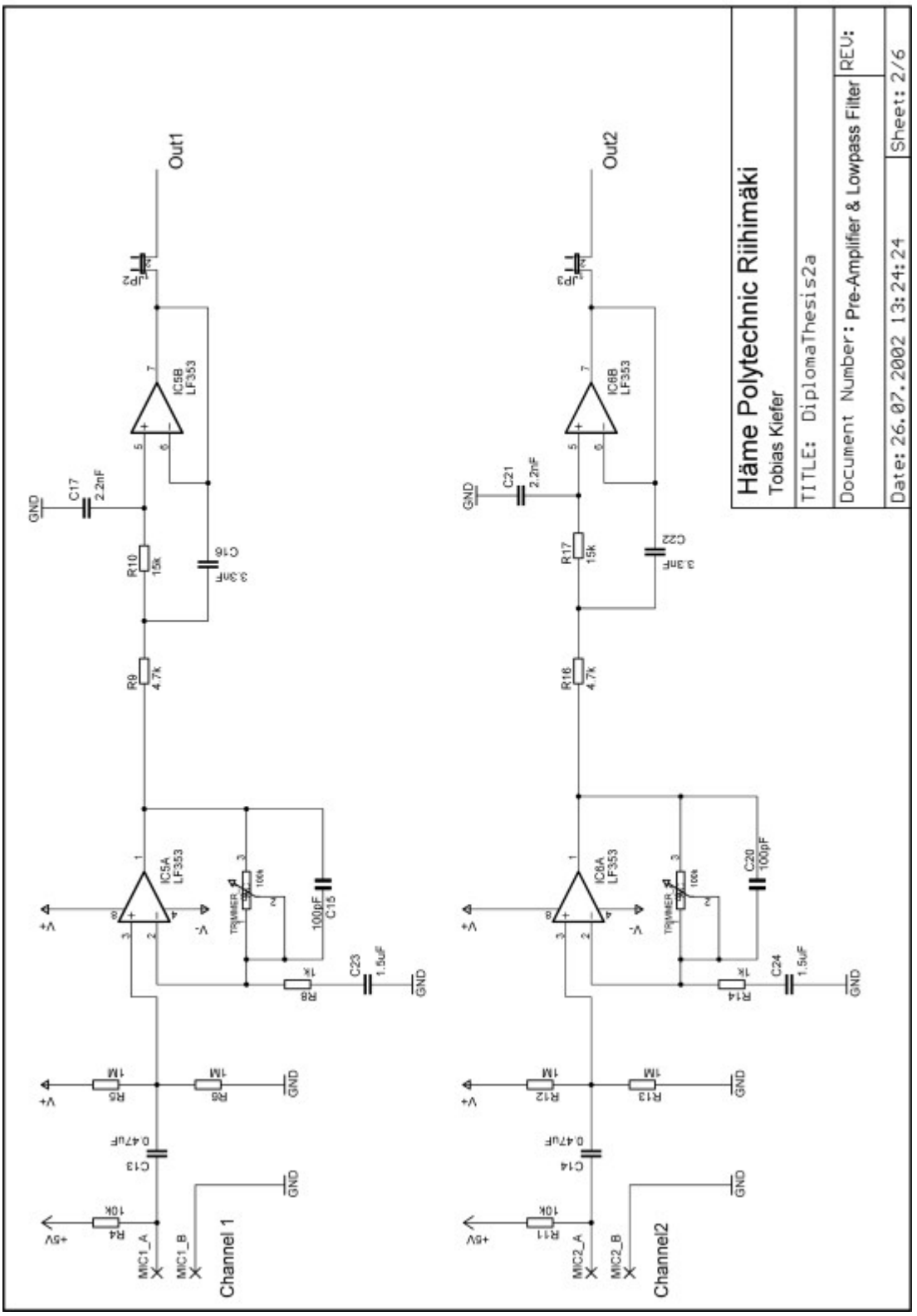
Using this IC means that the hardware part would be enormously reduced and furthermore a FIR bandpass filter has to be programmed. The calculation of the filter's coefficients is described in Appendix D.

APPENDIX

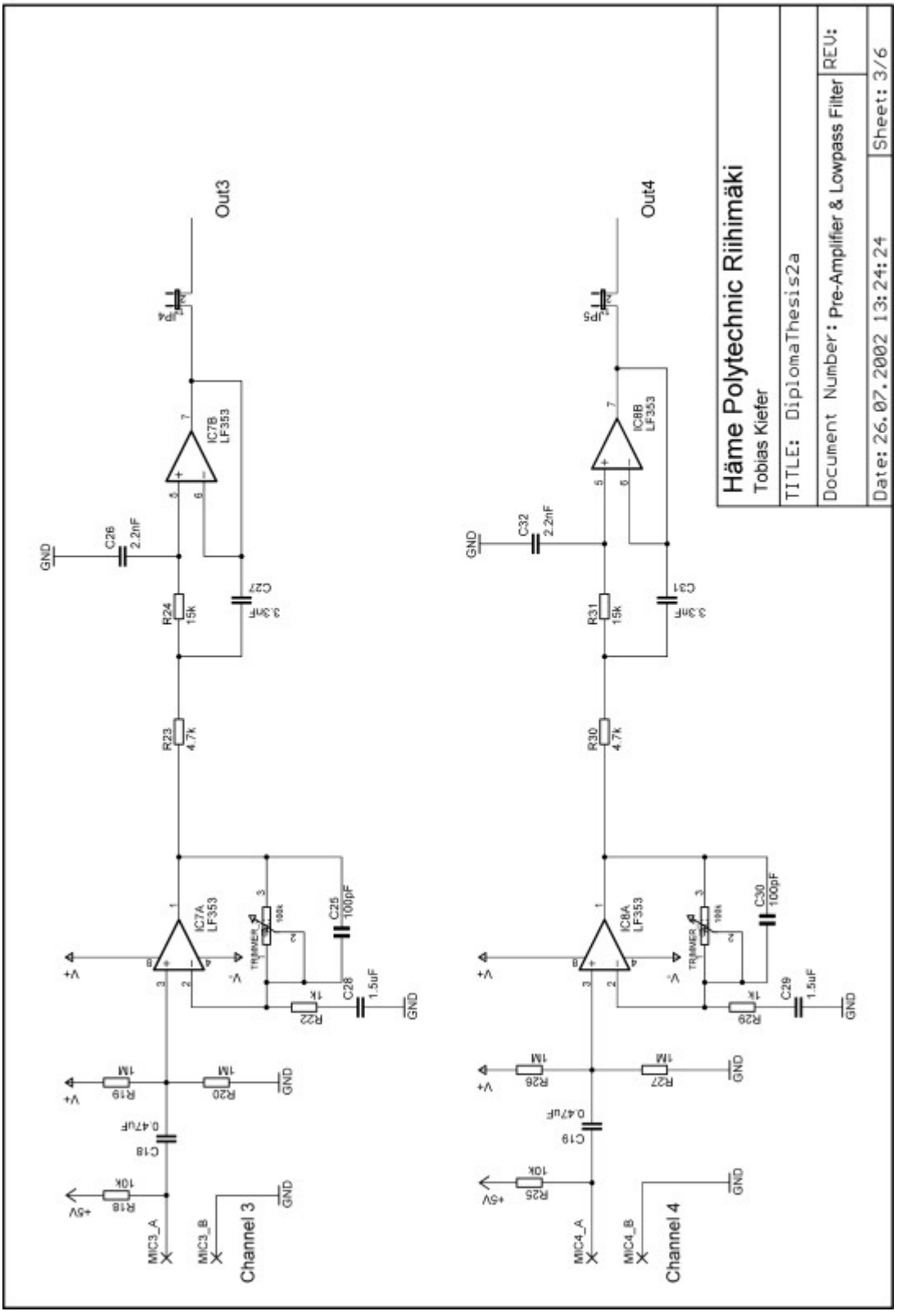
APPENDIX A - CIRCUIT DIAGRAMS



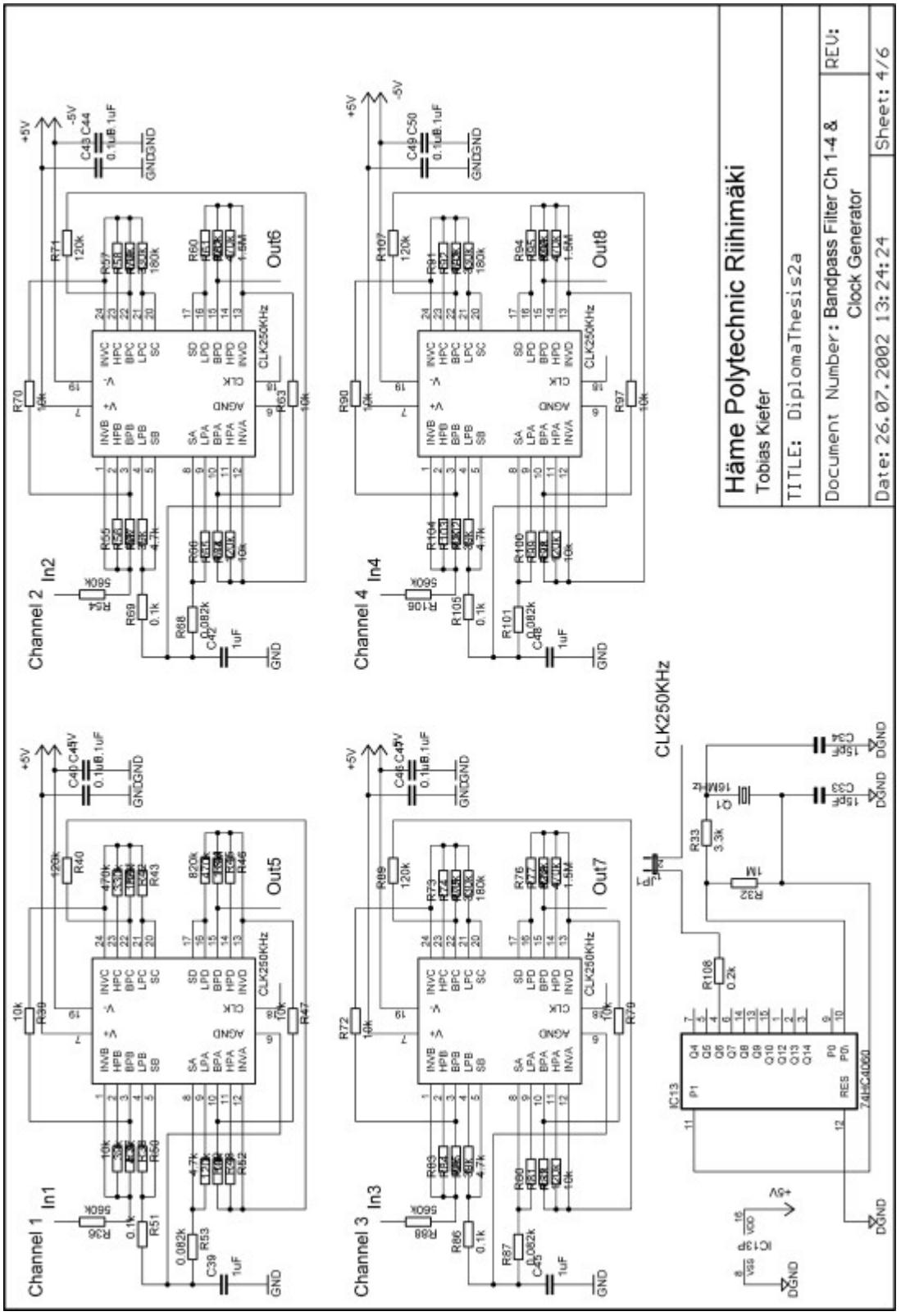
APPENDIX A - CIRCUIT DIAGRAMS



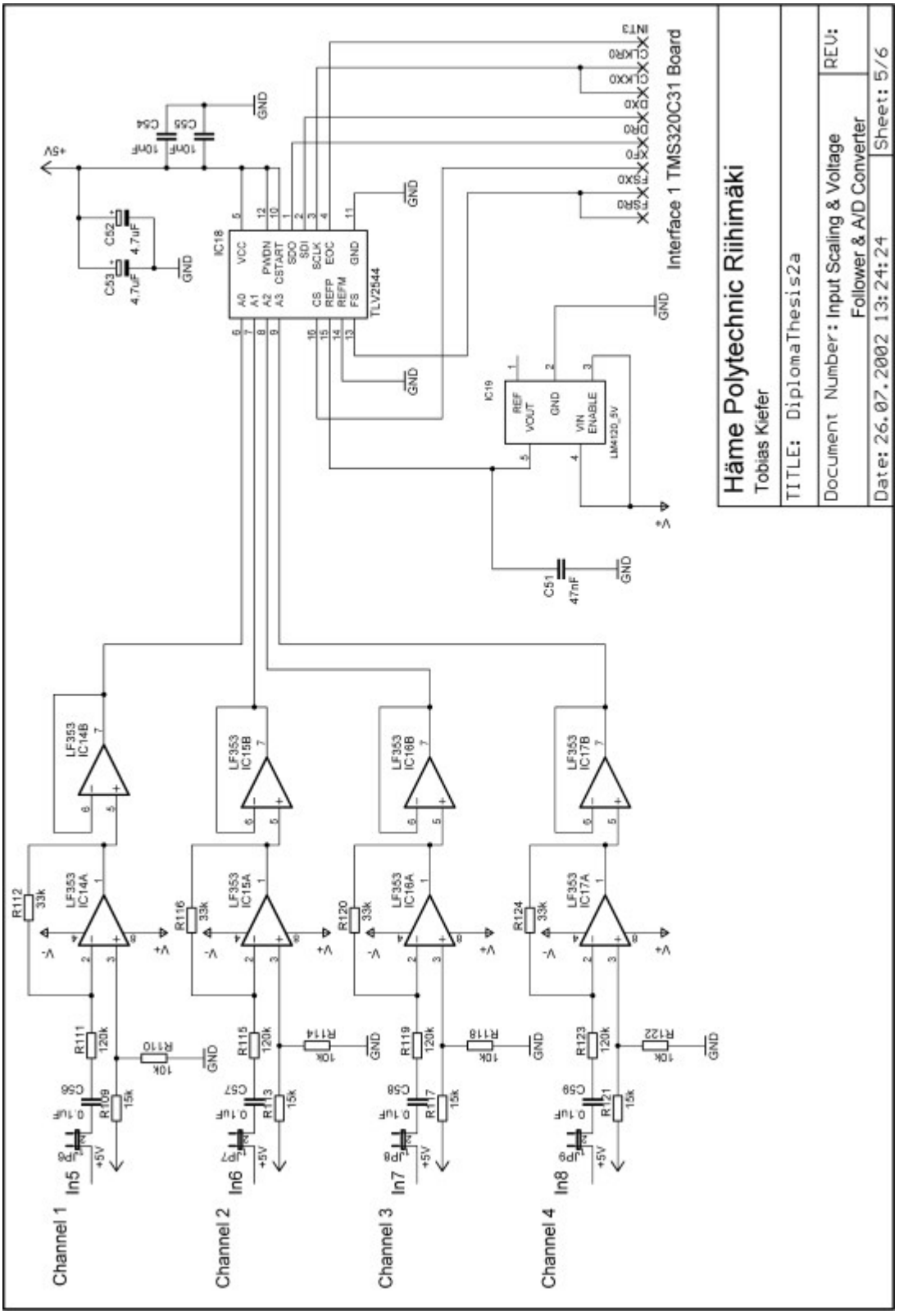
APPENDIX A - CIRCUIT DIAGRAMS



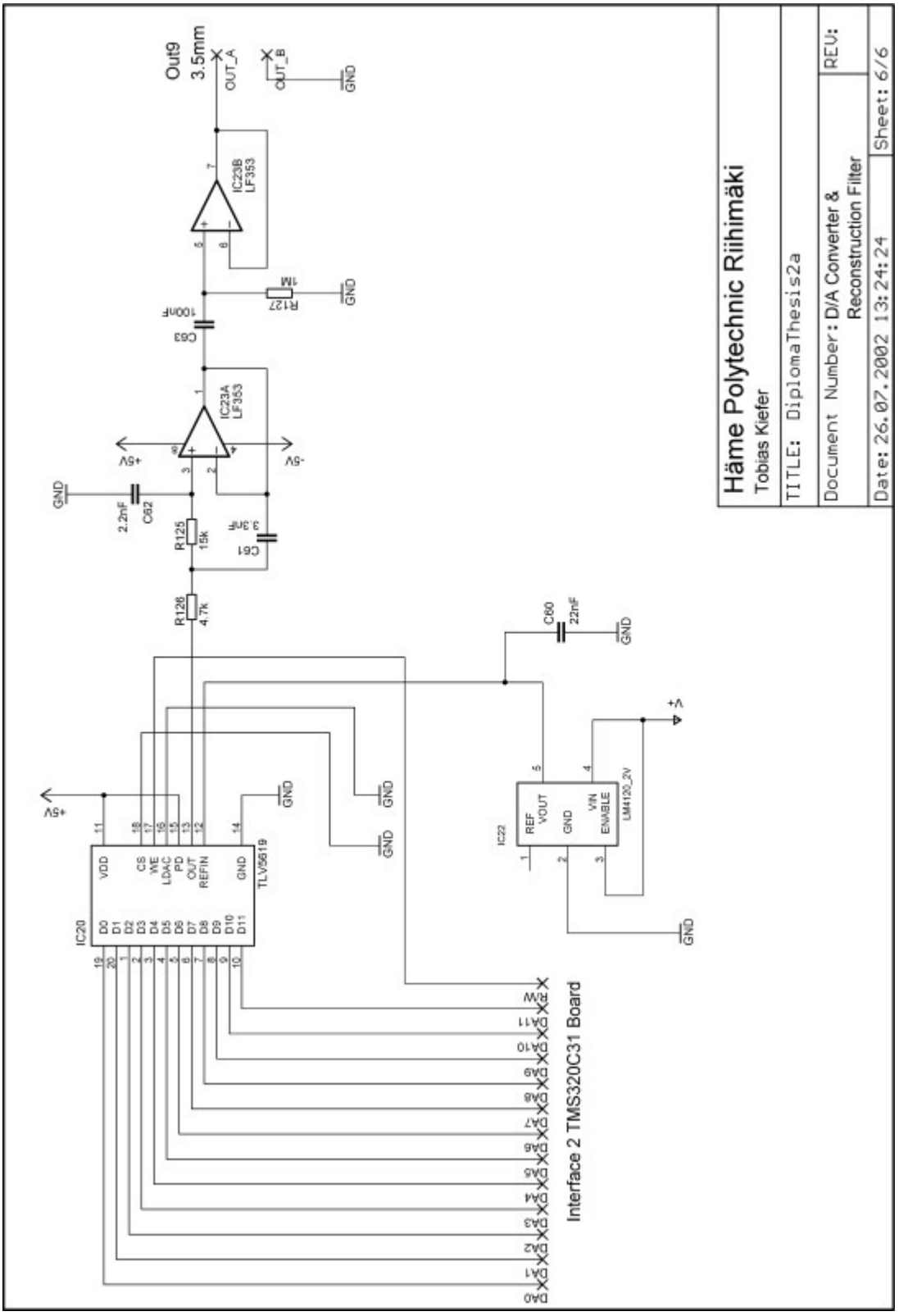
APPENDIX A - CIRCUIT DIAGRAMS



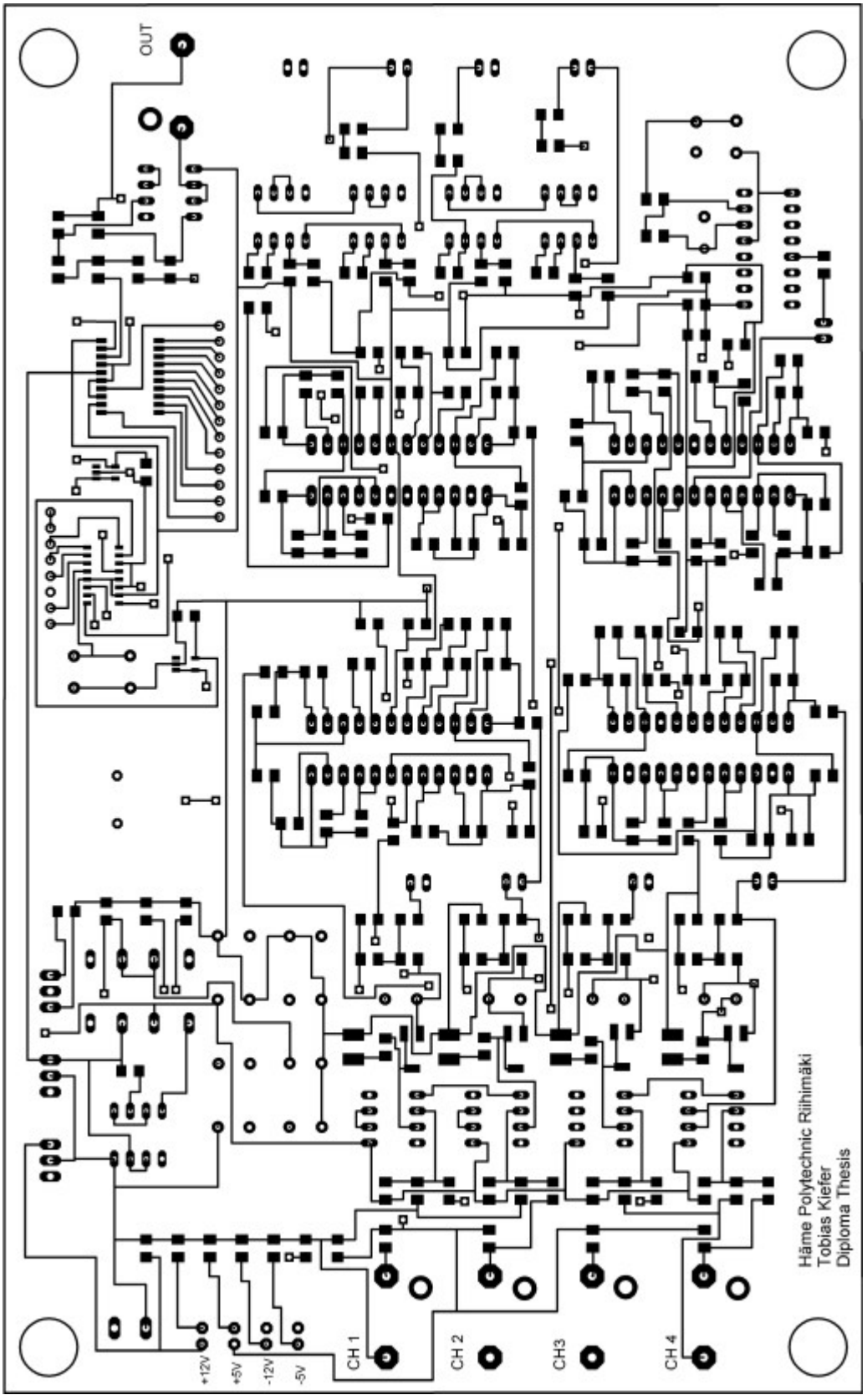
APPENDIX A - CIRCUIT DIAGRAMS



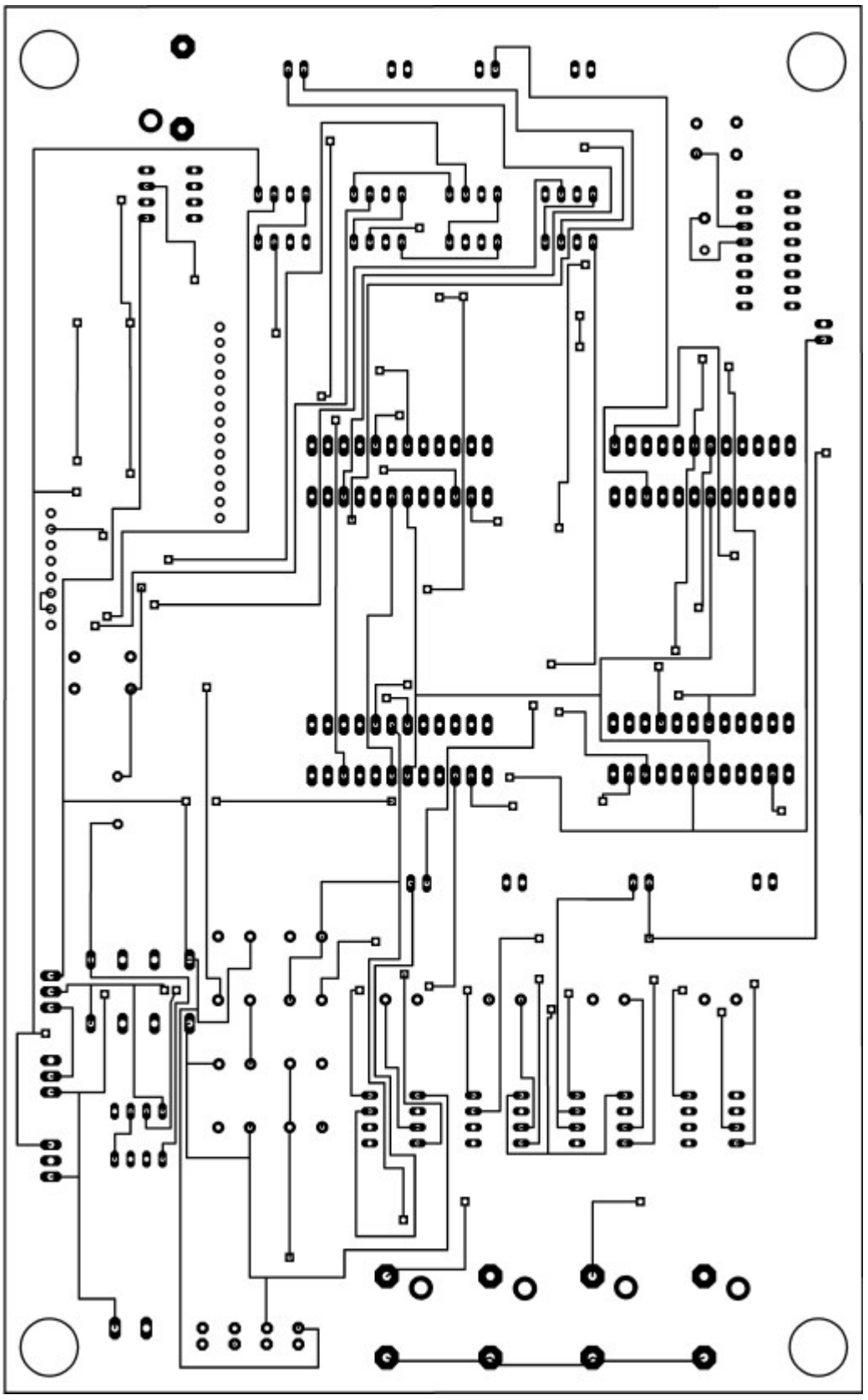
APPENDIX A - CIRCUIT DIAGRAMS



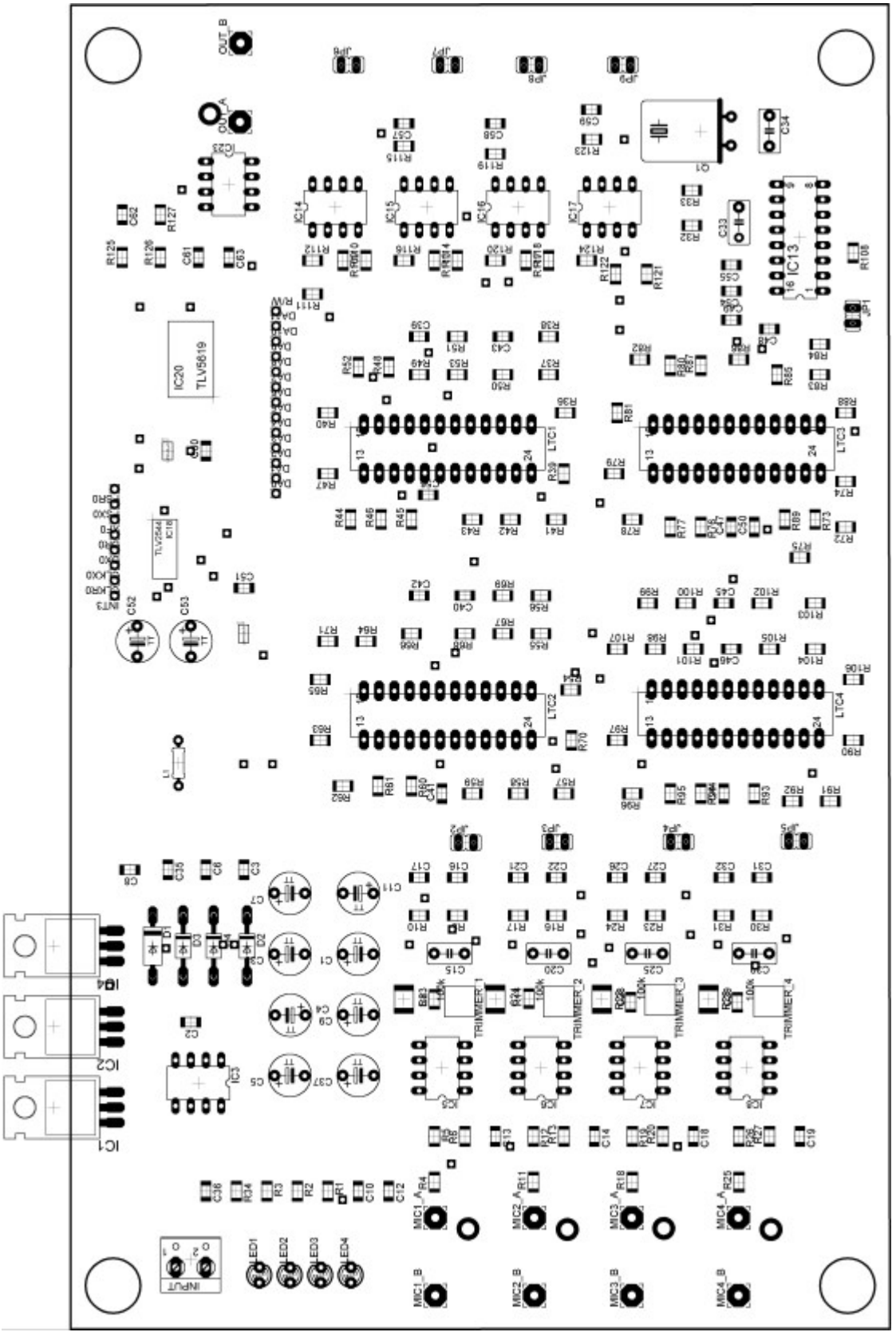
APPENDIX B - PRINTED CIRCUIT BOARD (PCB) LAYOUT



APPENDIX B - PRINTED CIRCUIT BOARD (PCB) LAYOUT



APPENDIX B - PRINTED CIRCUIT BOARD (PCB) LAYOUT



APPENDIX C - PART LIST

Item	Description	Identifier	Quantity
1	100 µF Electrolytic Capacitor	C1	1
2	0.1 µF SMD Capacitor	C2, C3, C6, C8, C10, C12, C35, C36, C40, C41, C43, C44, C46, C47, C49, C50, C56, C57, C58, C59	20
3	68 µF Electrolytic Capacitor	C4	1
4	4.7 µF Electrolytic Capacitor	C5, C7, C9, C11, C37, C38, C52, C53	8
5	0.47 µF SMD Electrolytic Capacitor	C13, C14, C18, C19	4
6	100 pF Capacitor	C15, C20, C25, C30	4
7	3.3 nF SMD Capacitor	C16, C22, C27, C31, C61	5
8	2.2 nF SMD Capacitor	C17, C21, C26, C32, C62	5
9	1.5 µF SMD Electrolytic Capacitor,	C23, C24, C28, C29	4
10	15 pF Capacitor	C33, C34	2
11	1.0 µF SMD Electrolytic Capacitor	C39, C42, C45, C48	4
12	47 nF SMD Capacitor	C51	1
13	10 nF SMD Capacitor	C54, C55	2
14	22 nF SMD Capacitor	C60	1
15	100nF SMD Capacitor	C63	1
16	Schottky Diode, 1N5817, 1 A	D1	1
17	Diode, 1N4004	D2, D3, D4	3
18	7812T Voltage Regulator	IC1	1
19	7805T Voltage Regulator	IC2	1
20	DC-DC Converter MAX765	IC3	1

APPENDIX C - PART LIST

Item	Description	Identifier	Quantity
21	7905T Voltage Regulator	IC4	1
22	Op-Amplifier LF353	IC5, IC6, IC7, IC8, IC14, IC15, IC16, IC17, IC23	9
23	SC Bandpass Filter LTC1068	IC9, IC10, IC11, IC12	4
24	Binary Counter 74HC4060	IC13	1
25	A/D Converter TLV2544	IC18	1
26	5 V Reference Voltage LM4120	IC19	1
27	D/A Converter TLV5619	IC20	1
29	2 V Reference Voltage LM4120	IC22	1
30	Jumper	J1,J2, J3, J4, J5, J6, J7, J8, J9	9
31	47 µH Inductor	L1	1
32	3mm LED, red	LED1, LED2, LED3, LED4	4
33	3.5 mm Mono Jack	Mic1,Mic2, Mic3, Mic4, Output	5
34	16 MHz Crystal	Q1	1
35	680 Ω SMD Resistor	R1	1
36	1.5 kΩ SMD Resistor	R2	1
37	330 Ω SMD Resistor	R3	1
38	10 kΩ SMD Resistor	R4, R11, R18, R25, R37, R39, R47, R52, R55, R63, R64, R70, R72, R79, R82, R83, R90, R97, R98, R104, R110, R114, R118, R122	24

APPENDIX C - PART LIST

Item	Description	Identifier	Quantity
39	1 MΩ SMD Resistor	R5, R6, R12, R13, R19, R20, R26, R27, R32, R127	10
40	1 kΩ SMD Resistor	R8, R14, R22, R29, R34	5
41	4.7 kΩ SMD Resistor	R9, R16, R23, R30, R49, R50, R66, R67, R80, R85, R100, R102, R126	13
42	15 kΩ SMD Resistor	R10, R17, R24, R31, R109, R113, R117, R121, R125	9
43	3.3 kΩ SMD Resistor	R33	1
44	560 kΩ SMD Resistor	R36, R54, R88, R106	4
45	39 kΩ SMD Resistor	R38, R56, R84, R103	4
46	120 kΩ SMD Resistor	R40, R48, R65, R71, R81, R89, R99, R107, R111, R115, R119, R123	12
47	470 kΩ SMD Resistor	R41, R45, R57, R61, R73, R77, R91, R95	8
48	330 kΩ SMD Resistor	R42, R58, R74, R92	4
49	180 kΩ SMD Resistor	R43, R59, R75, R93	4
50	820 kΩ SMD Resistor	R44, R60, R76, R94	4
51	1.5 MΩ SMD Resistor	R46, R62, R78, R96	4
52	100 Ω SMD Resistor	R51, R69, R86, R105	4
53	82 Ω SMD Resistor	R53, R68, R87, R101	4
54	200 Ω SMD Resistor	R108	1

APPENDIX C - PART LIST

Item	Description	Identifier	Quantity
55	33 kΩ SMD Resistor	R112, R116, R120, R124	4
56	100 kΩ SMD Trimmer	Trimmer1, Trimmer2, Trimmer3, Trimmer4	4
57	8 pin single row connector	Interface1 TMS320C31	1
58	13 pin single row connector	Interface2 TMS320C31	1

APPENDIX D - FIR BANDPASS FILTER

The coefficients C_n can be found for the following FIR bandpass filter using Figure D1, with the desired transfer function Hd(v) ideally represented: [15]

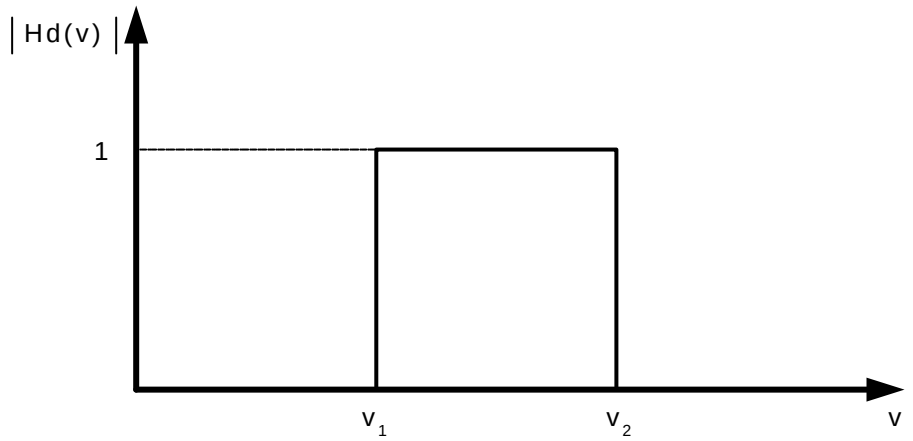


Figure D1 Desired Magnitude Transfer Function

Equation for the filter coefficients C_n:

$$C_n = \int_{v1}^{v2} Hd(v) * \cos(n\pi v)dv = \frac{\sin(n\pi v_2) - \sin(n\pi v_1)}{n\pi} \qquad \text{(D1)}$$

where v_1 and v_2 are the normalized cutoff frequencies, as shown in Figure D1.

with:

$$v = \frac{f}{F_N} \qquad \text{(D2)}$$

v = Normalized Frequency Variable

F_N = Nyquist Frequency

$$F_N = \frac{F_s}{2} \qquad \text{(D3)}$$

F_S = Sample Frequency

An alternative opportunity to find the coefficients for the FIR bandpass filter is using a program for digital filter development such as QEDesing 2000 or MatLab.

APPENDIX E - ABBREVIATIONS

Item	Acronym	Description
1	A/D	Analog to Digital
2	ADC	Analog to Digital Converter
3	ASR	Automatic Speech Recognition
4	C	Capacitor
5	CAD	Computer Aided Design
6	CLK	Clock
7	CLKR	Receive Clock Input
8	CLKX	Transmit Clock Input or Output
9	CMOS	Complementary Metal-Oxide-Silicon
10	CS	Chip Select
11	D/A	Digital to Analog
12	DAC	Digital to Analog Converter
13	DC	Direct Current
14	DR	Data Receive
15	DRC	Design Rule Check
16	DSP	Digital Signal Processor
17	DX	Serial Data Transmit
18	EOC	End Of Conversation
19	ESR	Effective Series Resistance
20	f_0	Center Frequency
21	f_c	Cutoff Frequency
22	f_{clk}	Clock Frequency
23	f_H	Higher Cutoff Frequency
24	f_L	Lower Cutoff Frequency
25	FIR	Finite Impulse Response
26	F_N	Nyquist Frequency
27	F_S	Sample Frequency
28	FS	Frame Synchronization

APPENDIX E - ABBREVIATIONS

Item	Acronym	Description
29	FSR	Receive Frame Register
30	FSX	Transmit Frame Register
31	G	Gain
32	GND	Ground
33	IC	Integrated Circuit
34	INT	Interrupt
35	INT3	External Interrupt
36	JP	Jumper
37	LDAC	Load Digital to Analog Converter
38	LED	Light Emitting Diode
39	MRA	Maximum Response Axis
40	OP-amp	Operational Amplifier
41	PBW	Pass band Width
42	PCB	Printed Circuit Board
43	PDIP	Plastic Dual-In-Line Packaging
44	PR	Pass band Ripple
45	Q	Crystal
46	R	Resistor
47	REFM	External Reference
48	REFP	External Reference
49	RSR	Receive Shift Register
50	SA	Stopband Attenuation
51	SBW	Stopband Width
52	SC	Switched Capacitor
53	SCLK	Input Serial Clock
54	SDI	Serial Data Input
55	SDO	Serial Data Output
56	SMD	Surface Mounted Device

APPENDIX E - ABBREVIATIONS

Item	Acronym	Description
57	SNR	Signal to Noise Ratio
58	V-	Negative Power Supply
59	V+	Positive Power Supply
60	V_{cc}	Positive Supply Voltage
61	V_{dd}	Positive Supply Voltage
62	VoIP	Voice over IP
63	V_p	Peak Voltage
64	XF	External Flags

Units:

Item	Acronym	Description
1	A	Ampere
2	dB	Decibel
3	F	Farad
4	H	Henry
5	Hz	Hertz
6	V	Volt

APPENDIX F - REFERENCES

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APPENDIX F - REFERENCES

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[15] R. Chassaing, Digital Signal Processing with C and the TMS320C30, John Wiley & Sons, Inc., page 105, (1992)

Used Datasheets:

- *7805 Voltage Regulator:* http://www.national.com/ds/LM/LM7512C.pdf
- *7812 Voltage Regulator:* http://www.national.com/ds/LM/LM7512C.pdf
- *7905 Voltage Regulator:* http://www.national.com/ds/LM/LM7905.pdf
- *MAX765:* http://www.maximic.com/samplescart.cfm?Action=Add&PartNo=MAX765
- *LF353 OP Amplifier:* http://www.national.com/ds/LF/LF353.pdf
- *LTC1068 SC Bandpass Filter:* http://www.linear.com/pdf/1068fa.pdf
- *MF10 SC Bandpass Filter:* http://pdfserv.maxim-ic.com/arpdf/MF10.pdf
- *74HC4060 Binary Counter:* http://www.fairchildsemi.com/ds/MM/MM74HC4060.pdf
- *TLV2544 A/D Converter:* http://www-s.ti.com/sc/ds/tlv2544.pdf
- *TLV5619 D/A Converter:* http://www-s.ti.com/sc/ds/tlv5619-ep.pdf
- *LM4120 Reference Voltage:* http://www.national.com/ds/LM/LM4120.pdf